IC Synthesis and Optimization Challenges and Solutions

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Overview

- Synthesis and Optimization Challenges and Solutions on the example of 90nm EDK
- Overview of 90nm EDK content

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90nm EDK: Solution for Challenges

- Anticipated for the use of educational purposes
- Free from intellectual property restrictions EDK
- Foreseen to support
  - Advanced design methodologies
    - Design complexity challenges
    - Design For Manufacturing (DFM)
  - Capabilities of SYNOPSYS tools
- Anticipated for designing complex ICs (processors)

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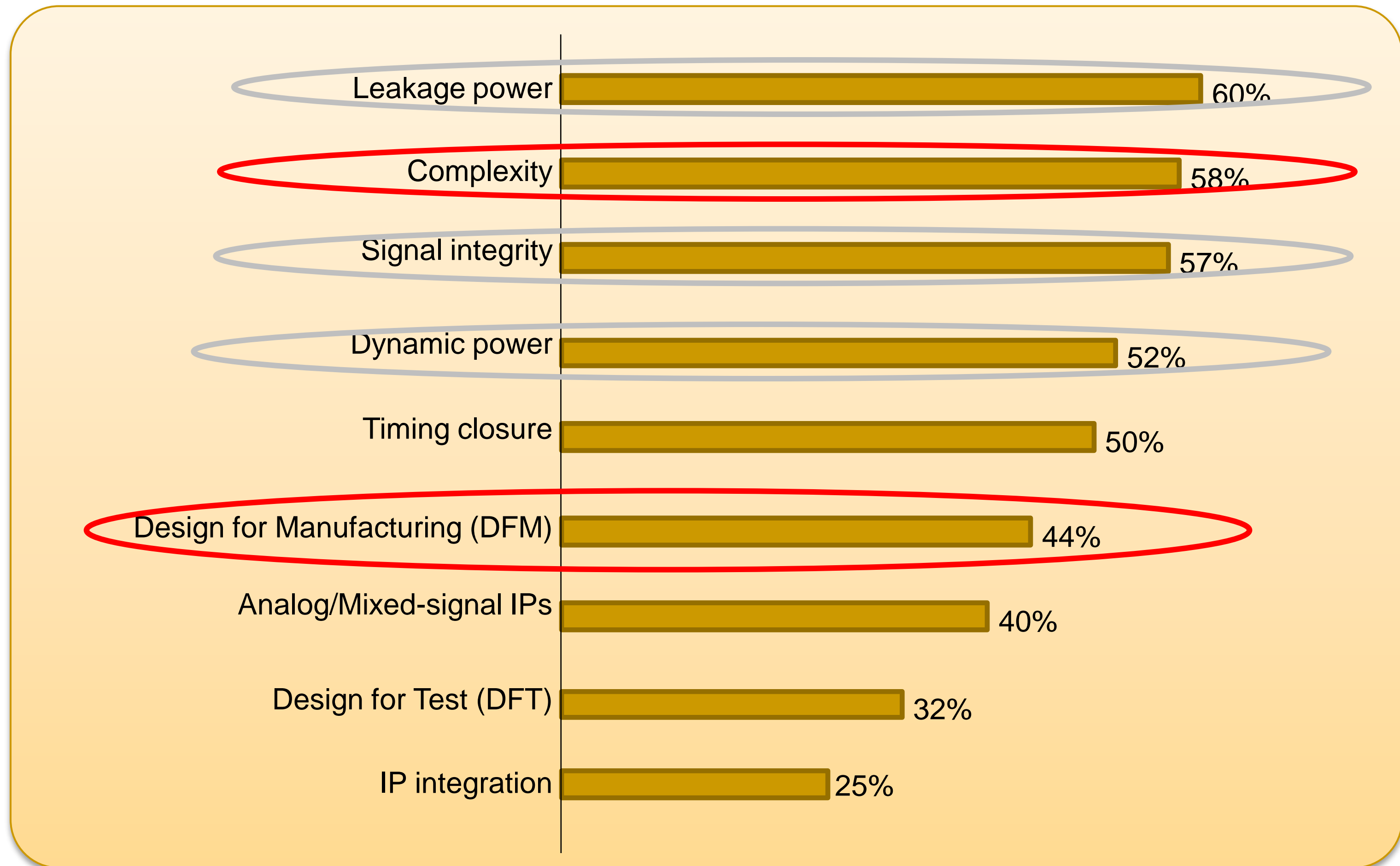
IC Design Challenges



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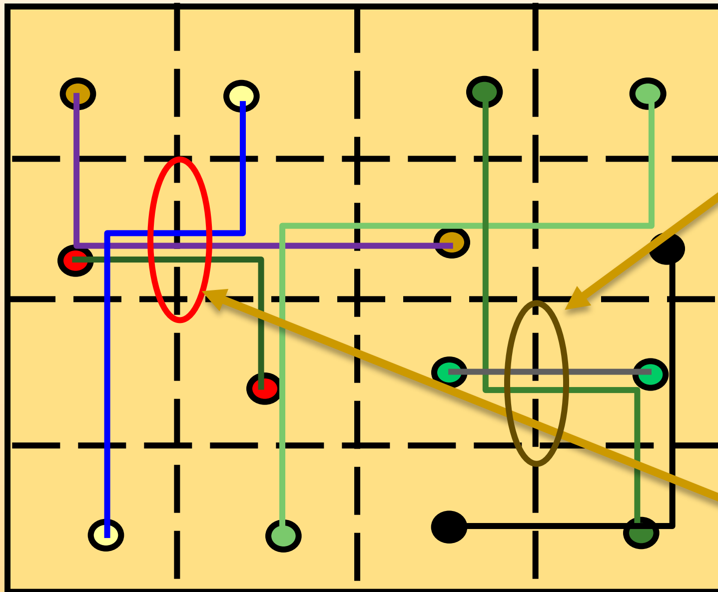
Routing Congestion

Routing resources < *Routing Requirements* → *Congestion*



Routing requirement = 2
Routing resource = 2
overflow = 2 - 2 =0→ No Congestion

Routing requirement = 3
Routing resource = 2
overflow = 2 - 3 = -1 → Congestion

Requires Congestion-Aware Placement

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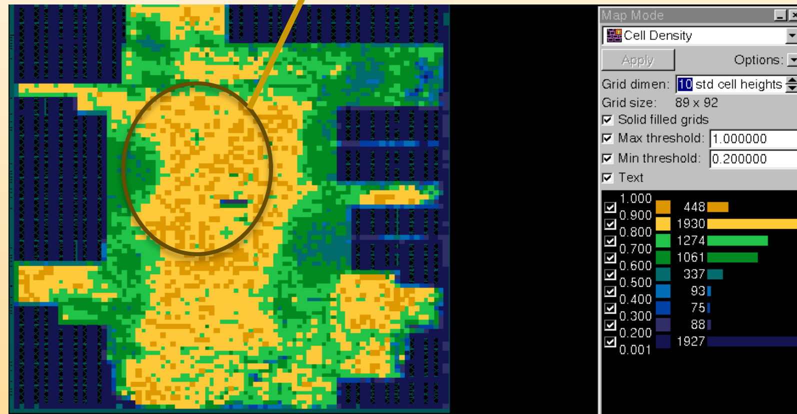
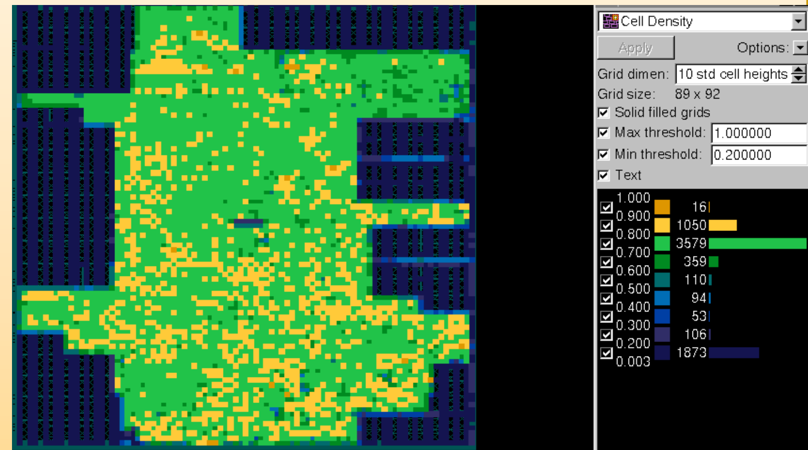
Congestion Map

High congestion regions



Uniform density



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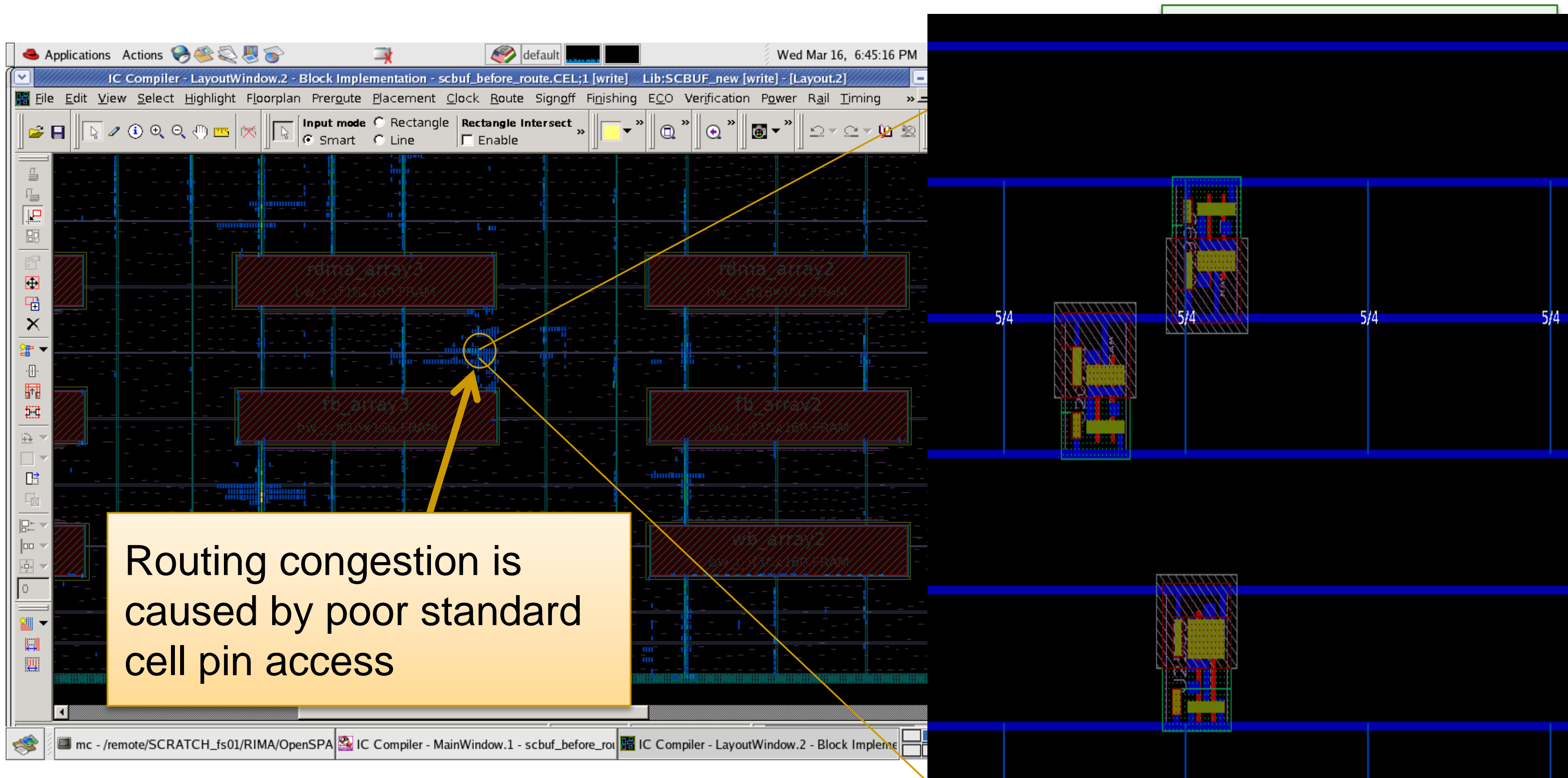
Congestion in Standard Cell Placement regions



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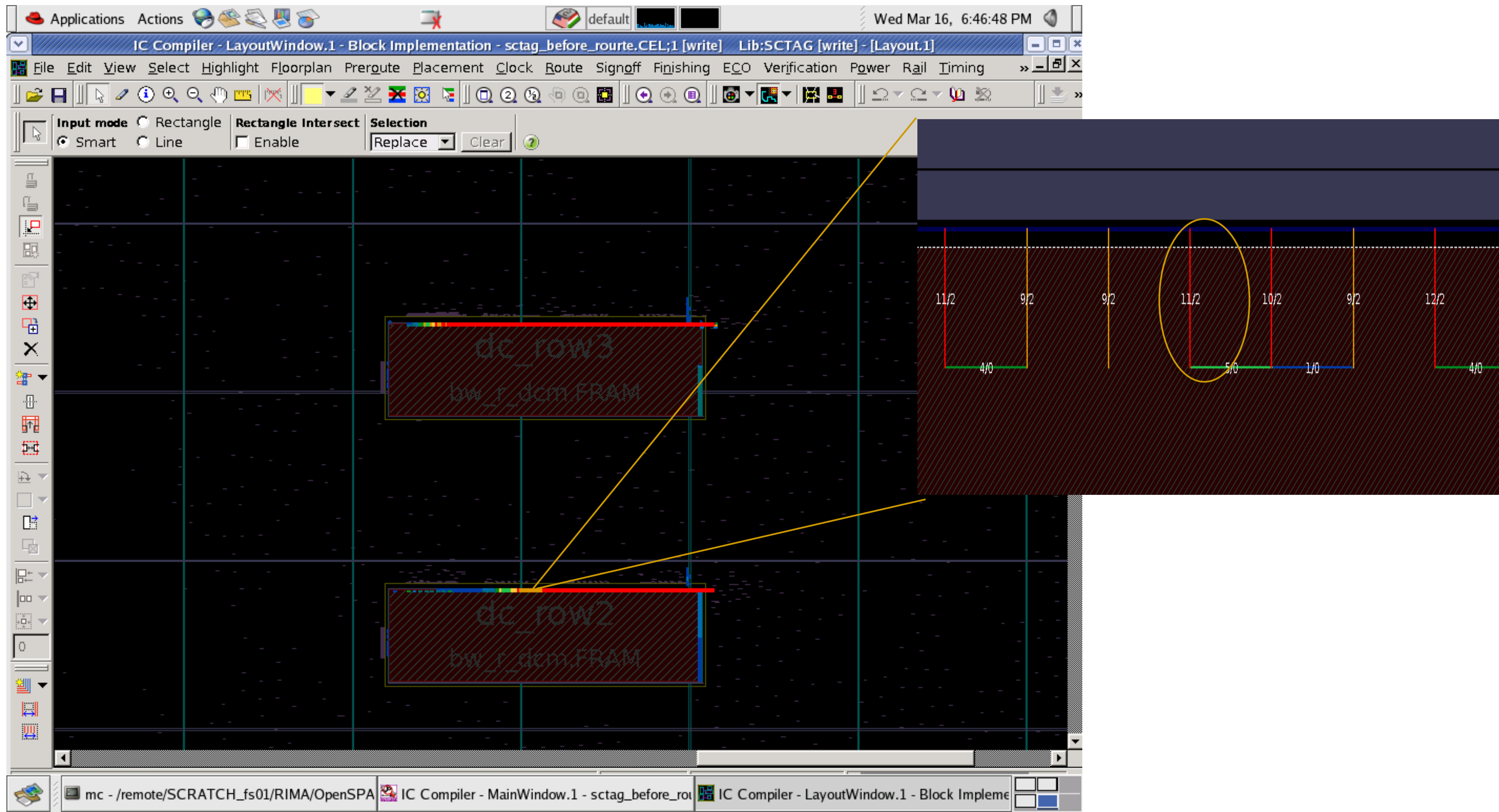
Congestion Caused by Poor Pin Acessibility



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Sources of Congestion and Solutions

- High placement density
  - Too much routing required on small area
  - Solution: less dense placement
- Bad standard cell and IP pin access
  - Bad pin placement causes congestion
  - Solution:
    - Increase IP pin access
    - Increase standard cell pin access

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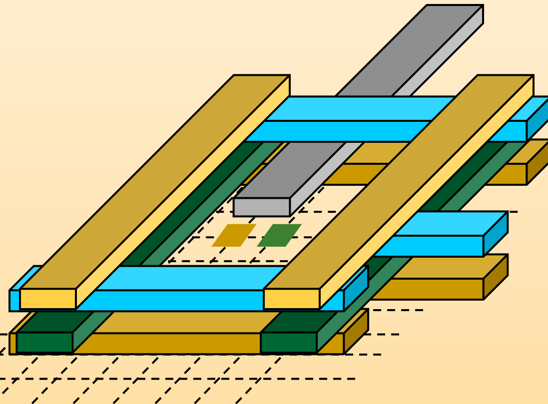
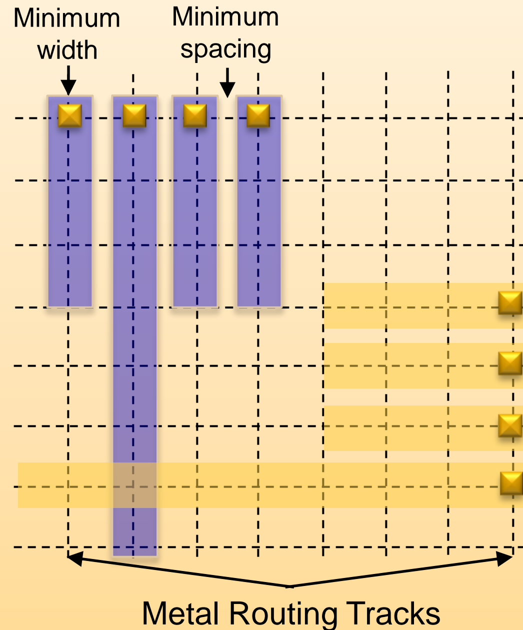
Routing Resource

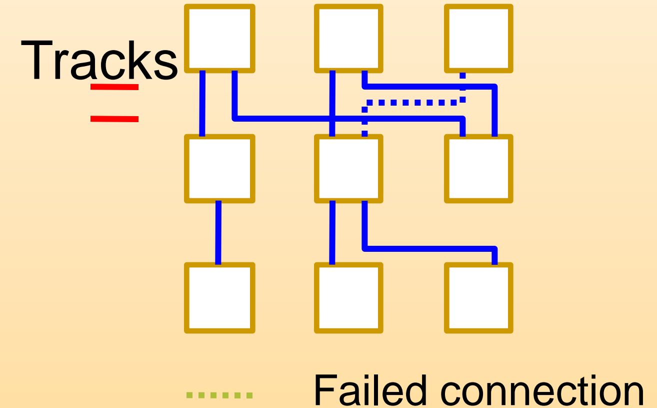
Layers have perpendicular directions

Routing is done on tracks

Insufficient number of tracks bring congestion







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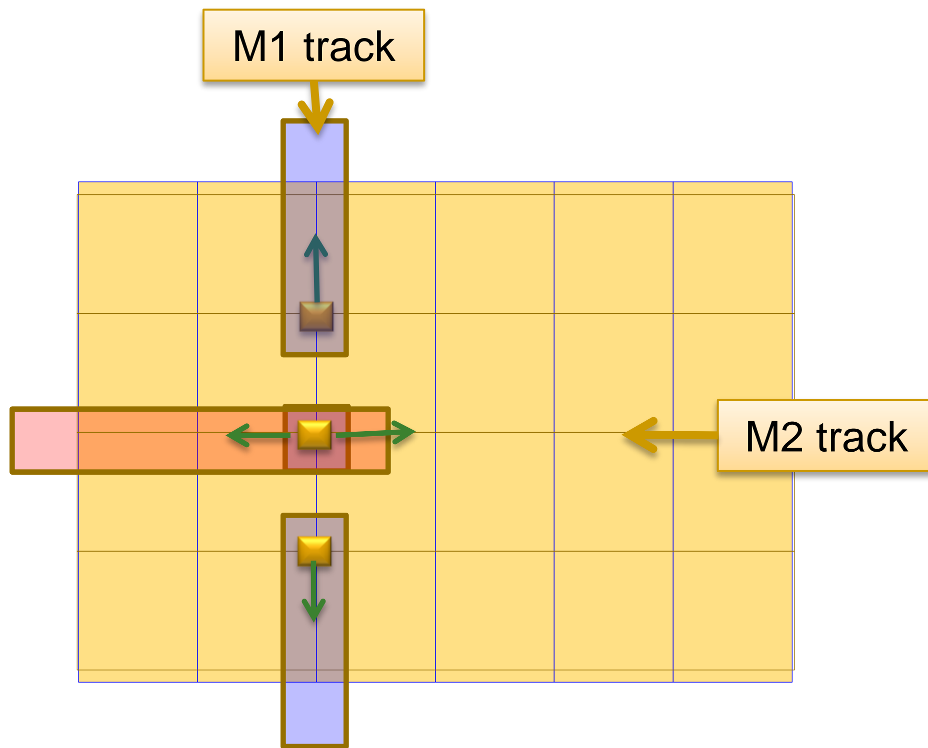
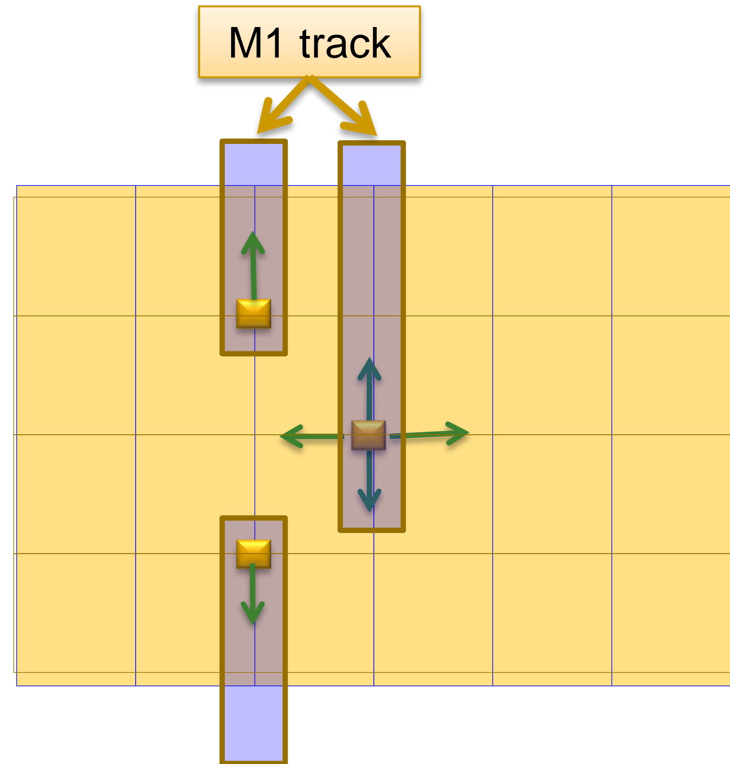
Standard cell routability improvement





If pins are placed on same track additional M2 routing resources spent

Routing can be accomplished using only M1

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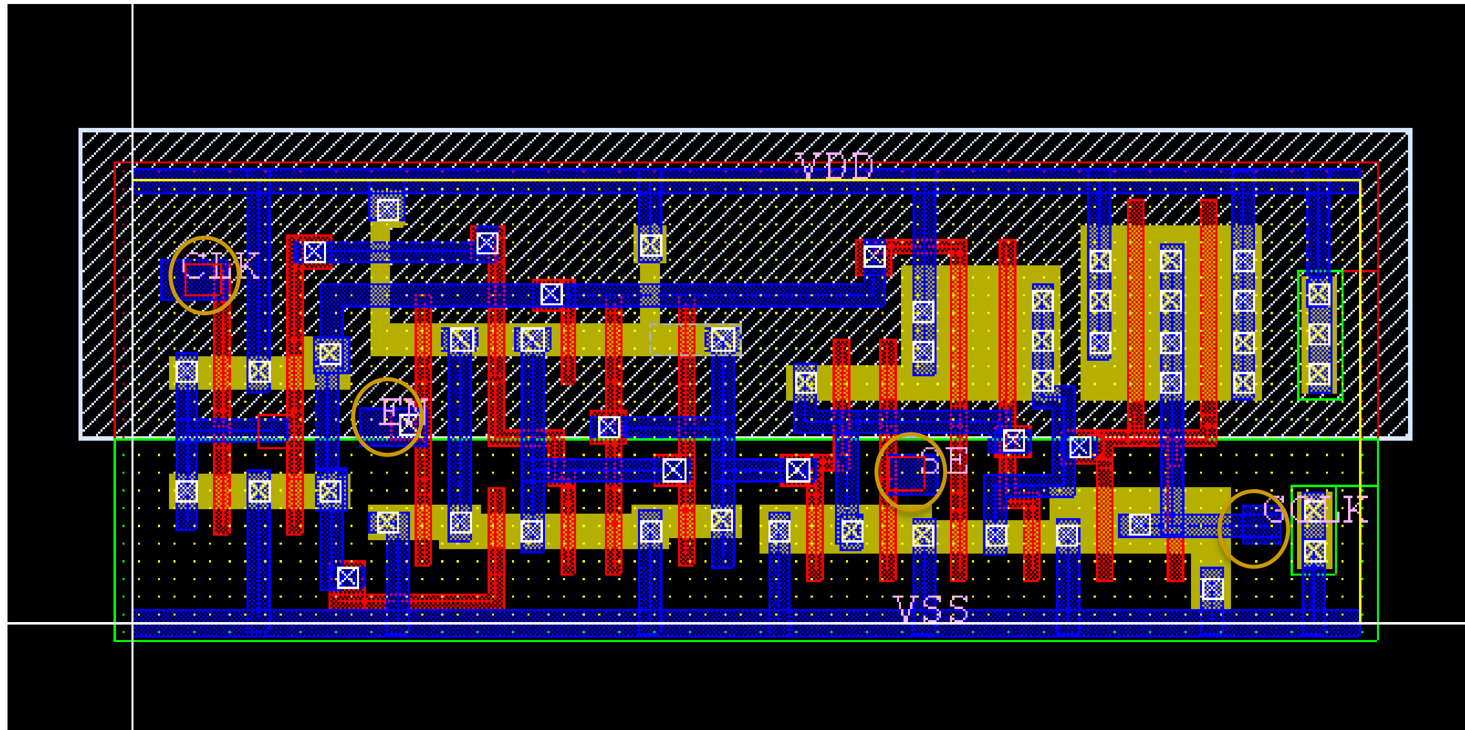
90nm EDK: Standard Cell Physical Design



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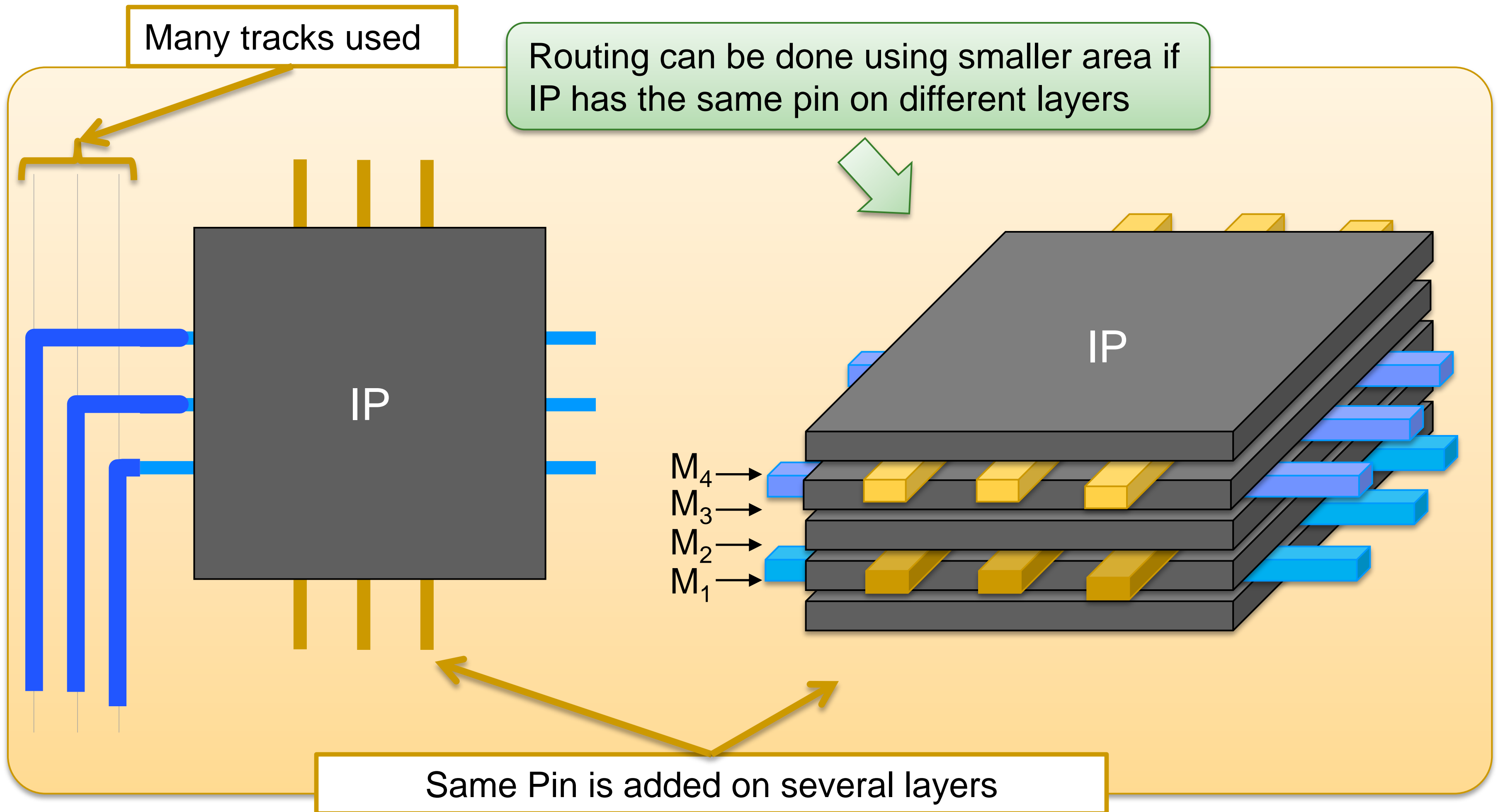
IP Pin Access Improvement



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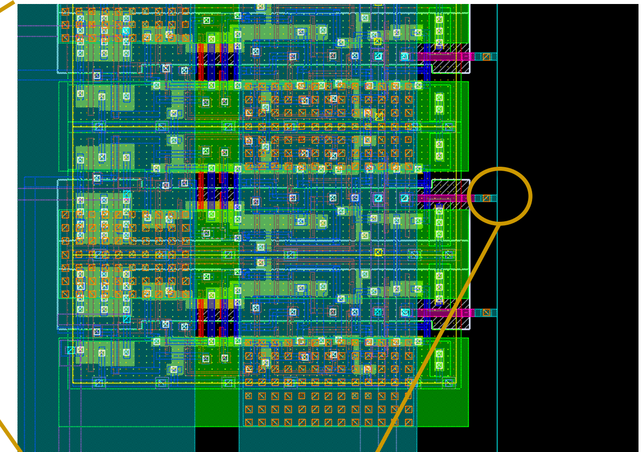
90nm EDK: Memory Cell



Pin available on M3 and M5 layers

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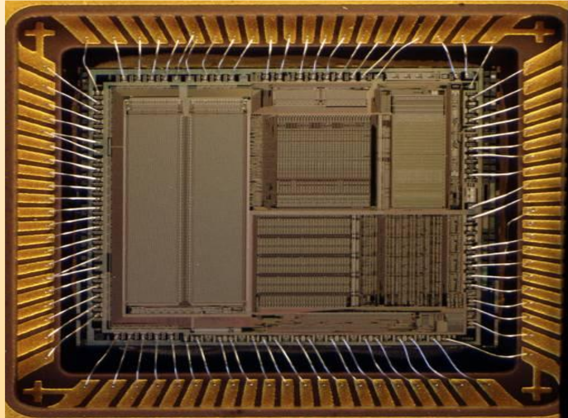
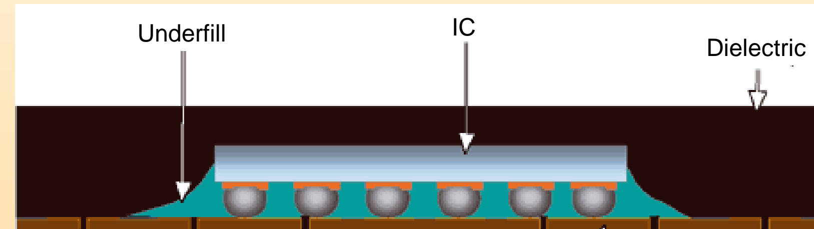
Advanced I/O Cell Placement

Wire Bond



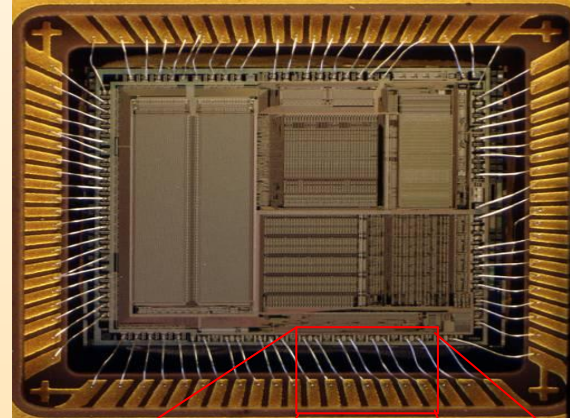
Flip-Chip

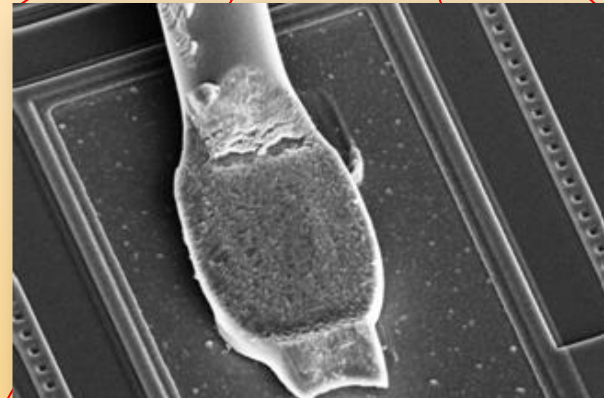


Wire Bond

- Most widespread method
- IC is connected with package pins with thin wires

Wire Bonding Example





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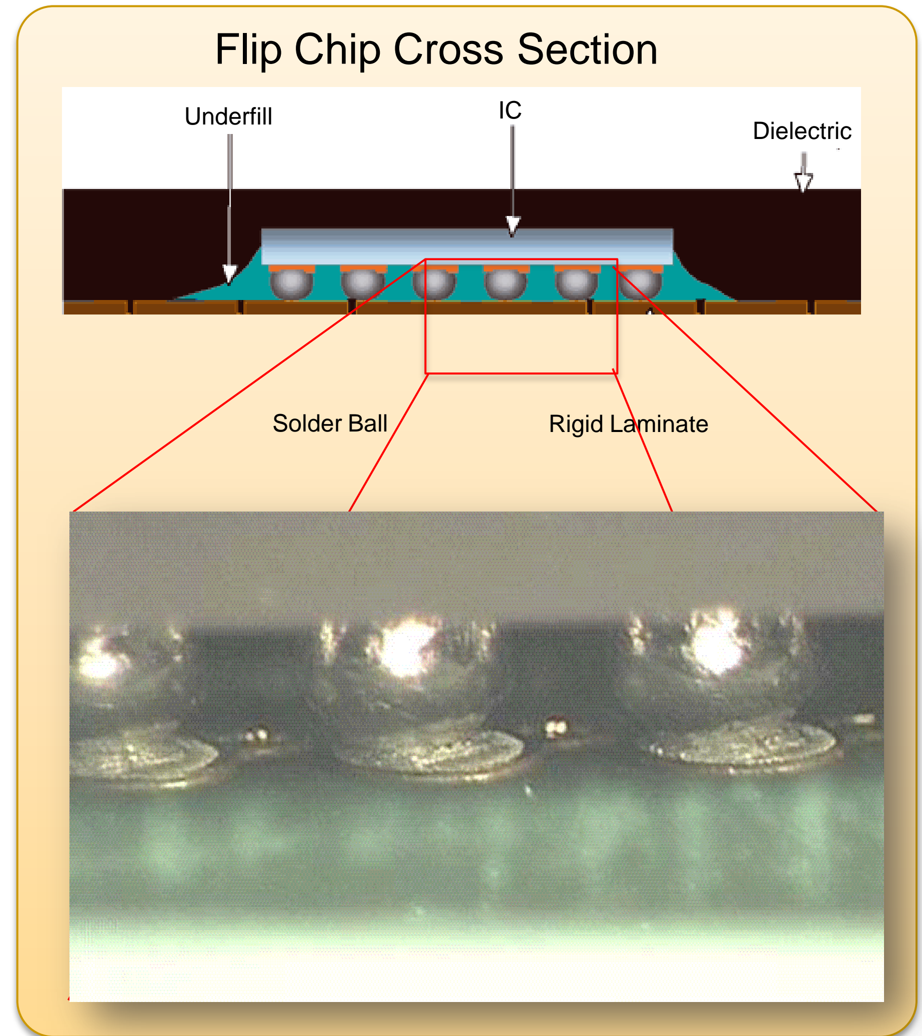
Flip-Chip

- Modern method of the I/O connection
- IC is connected with package using solder balls



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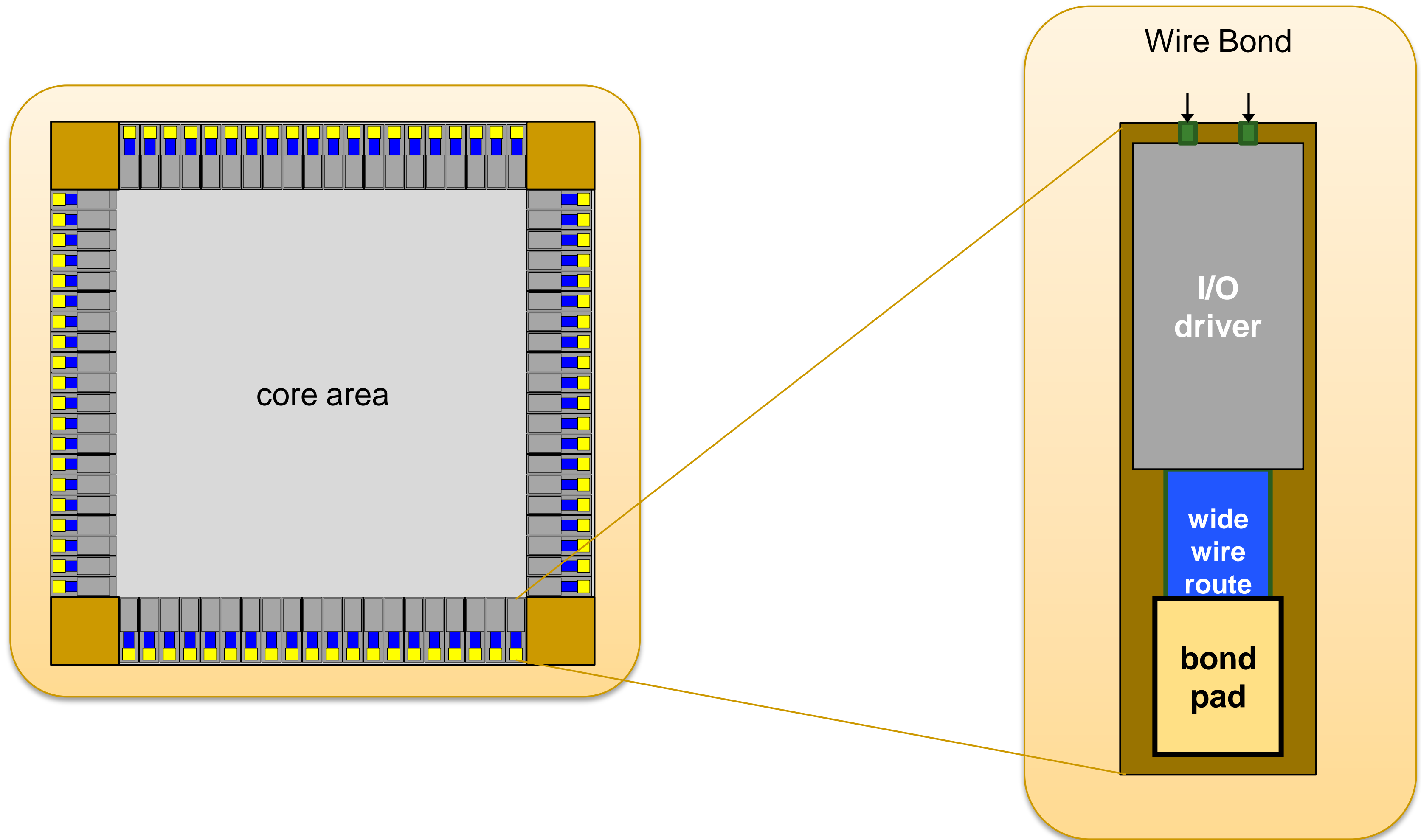
Wire Bond Placement



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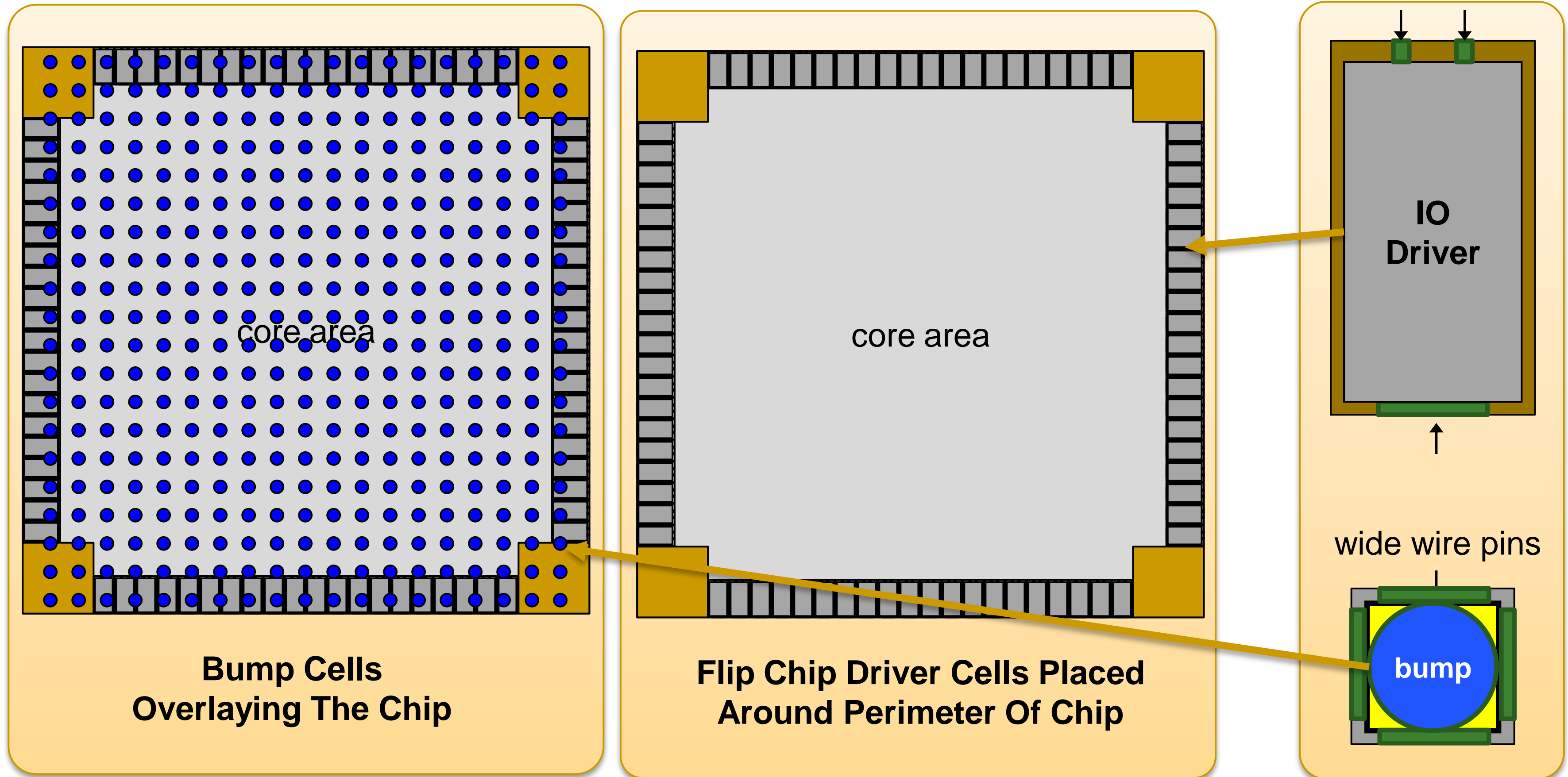
Flip Chip Placement



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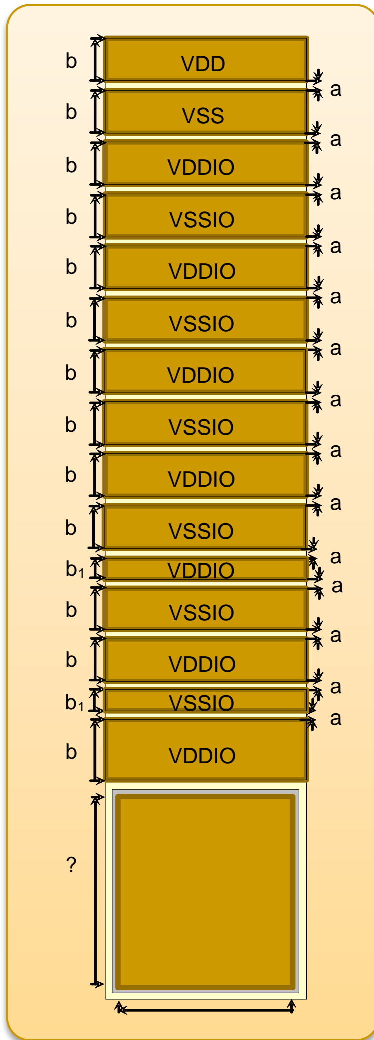
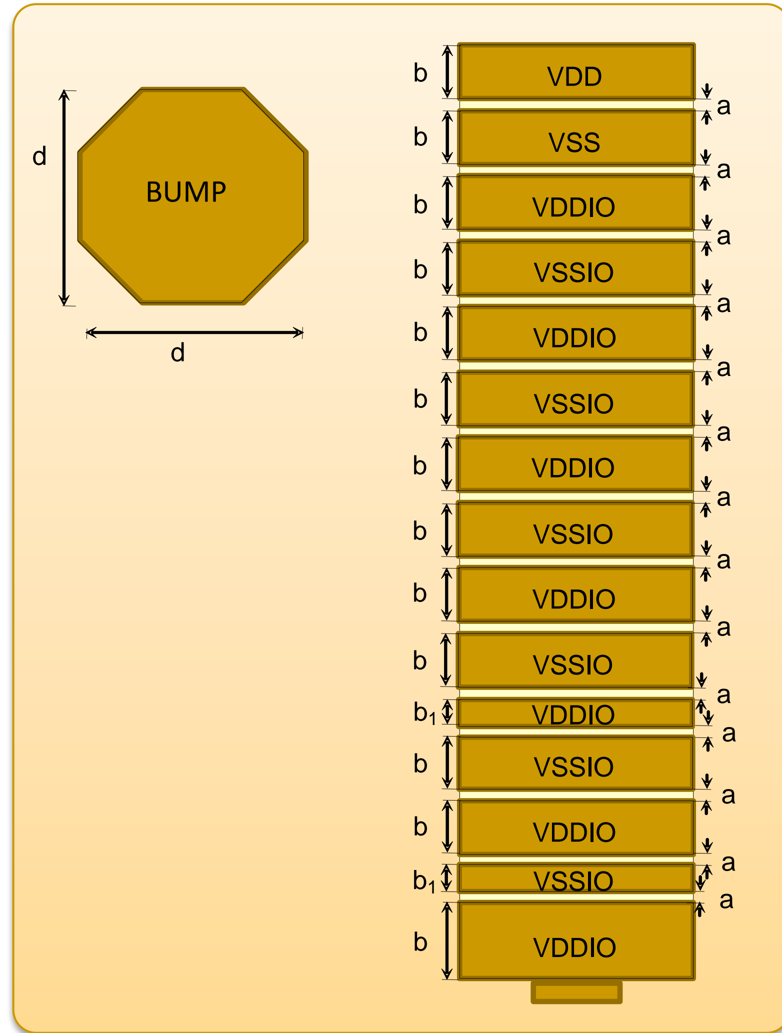
I/O Cell Physical Structures





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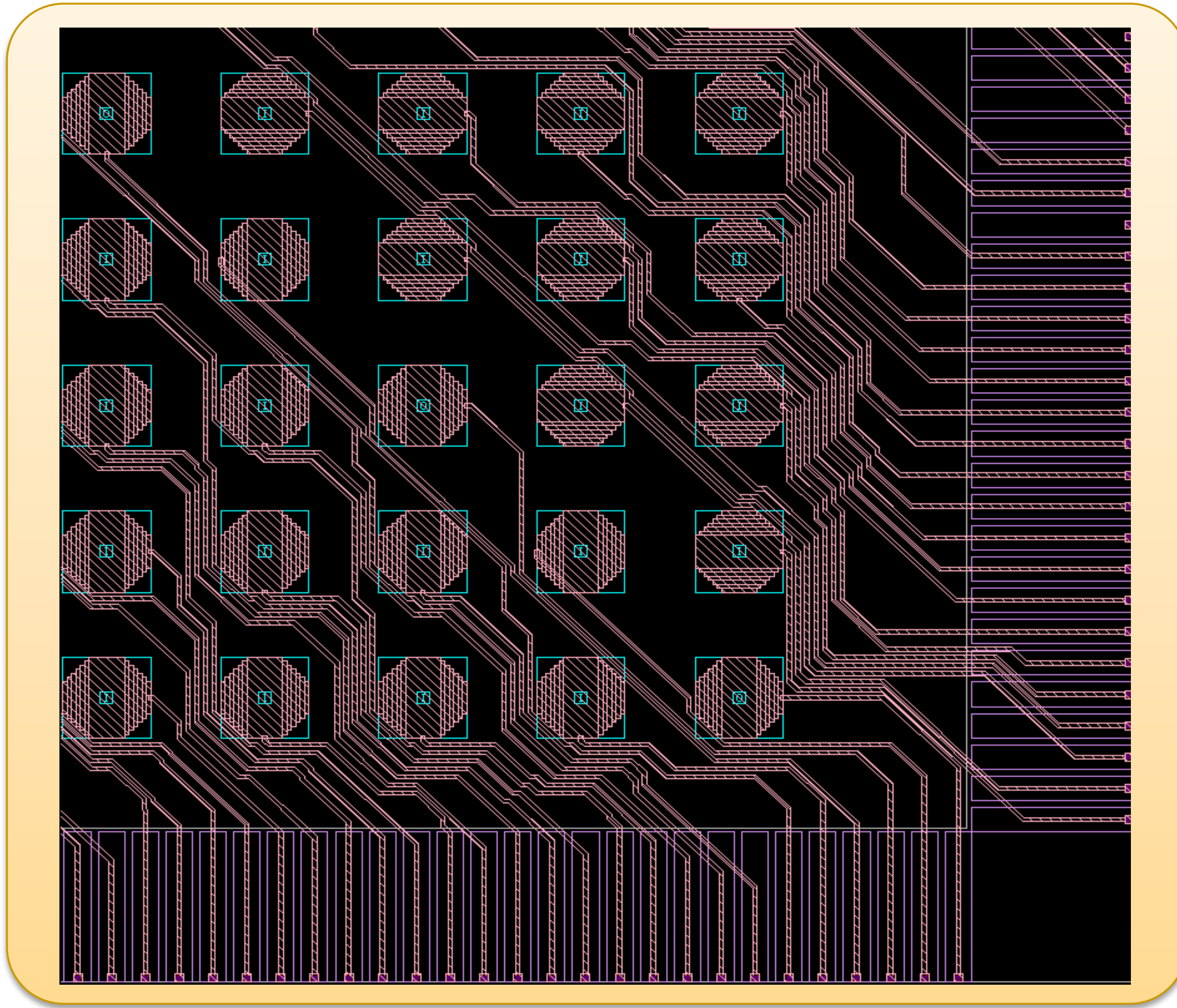
Flip-Chip Routed Example



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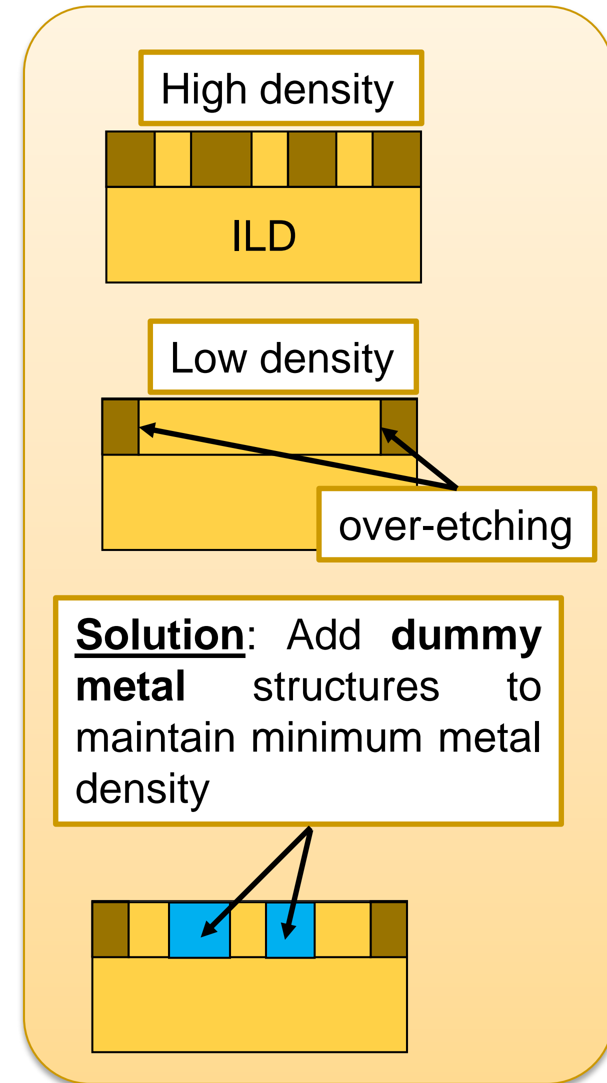
Metal Density

- Metal Density
  - Min density
    - ~30%
    - Dummy metal structures required to add metal
  - Max density
    - ~80%
    - Wide wires should be converted into parallel lines



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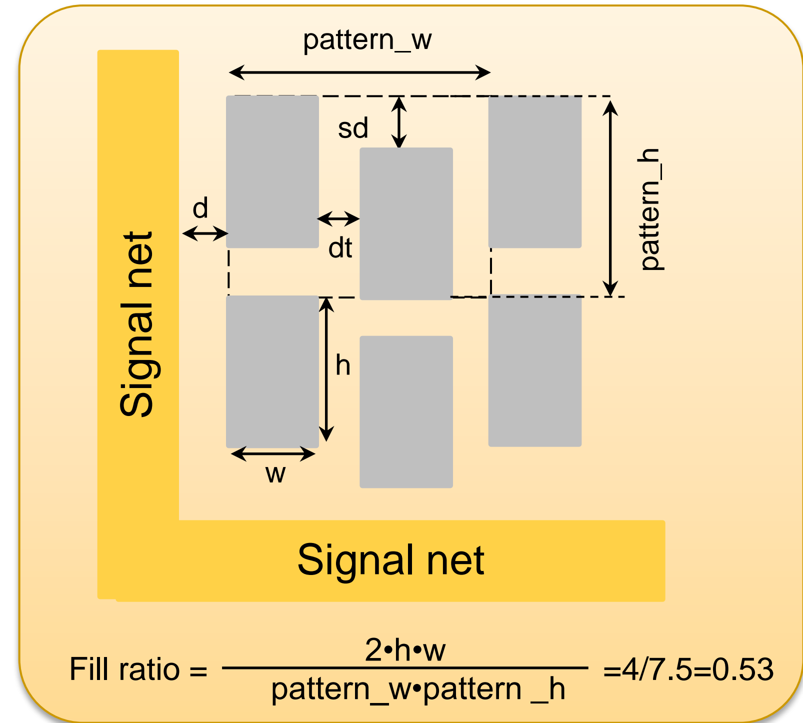
Dummy Metal Fill Utility

- For SAED 90nm EDK density fill utility was created (based on Synopsys IC Validator)
  - Automatically fills low density spaces with dummy “tiles”
  - Brings design to around 53% density (when min is 30% and max is 80%)



Description	μm	Mark
Tile width	1	w
Tile height	2	h
Tile spacing to signal net	0.5	d
Tile spacing	0.5	dt
Minimum stagger dist	0.5	sd
Fill pattern width	3	pattern _w
Fill pattern height	2.5	pattern _h

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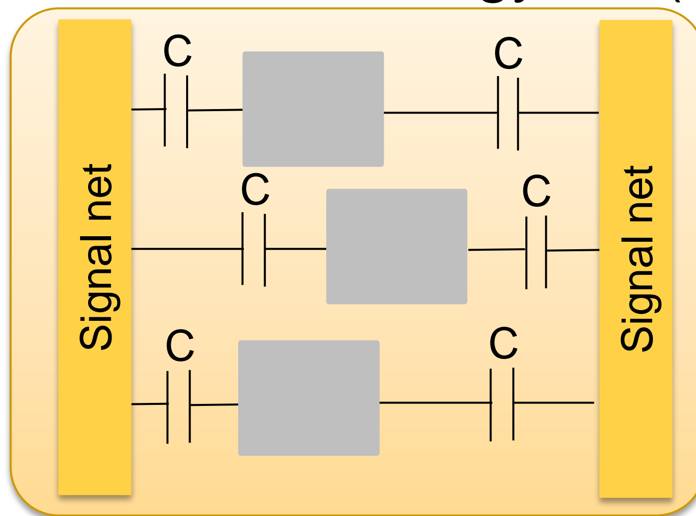
Metal Fill Extraction Problem

- Extracting metal fill objects is runtime and memory consuming
- Approximation of capacitive effects can be made
- StarRC provides Metal fill estimation capability in interconnect technology file (ITF).



Thousands of dummy tiles could make extraction run for hours!

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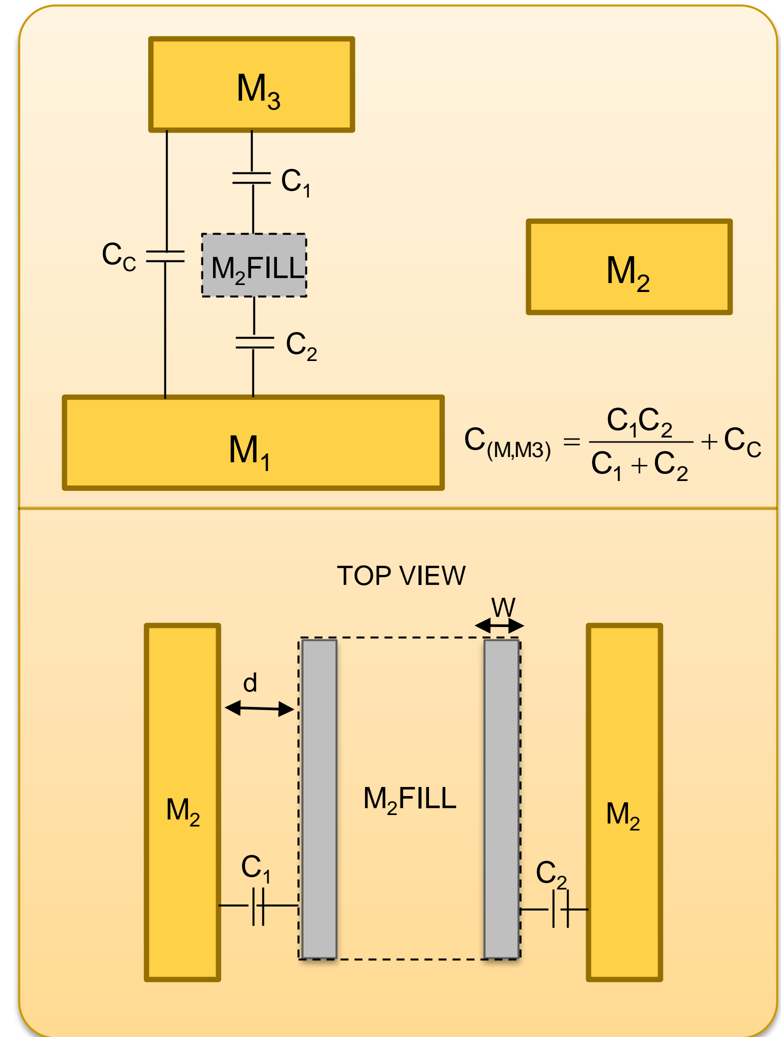
Metal Fill Estimation

- Metall fill estimation ITF was created
- Evaluation shows 13% difference in between estimated and real results



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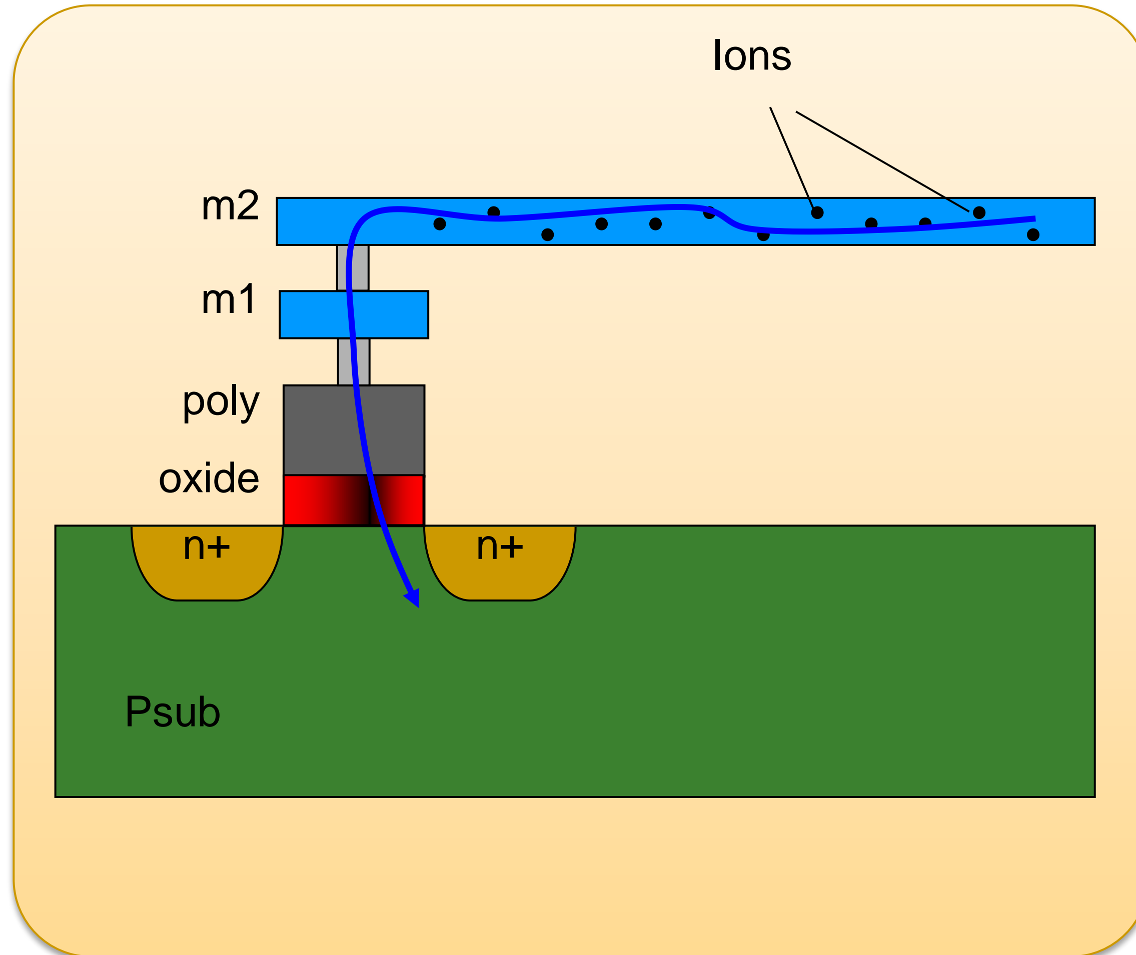
Antenna Effect



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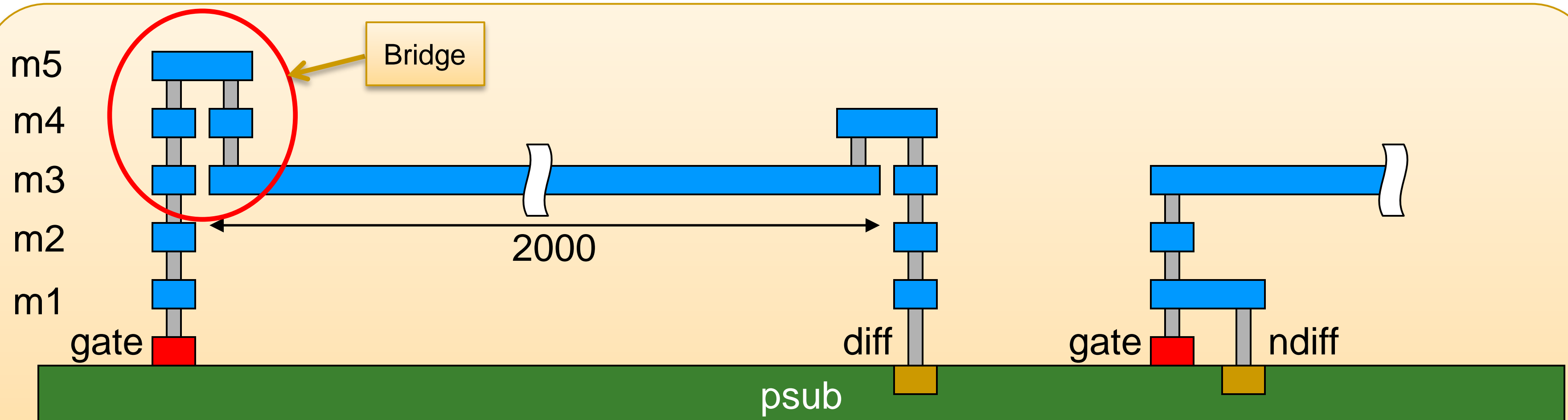
Antenna Fixing

- Two solutions: bridging and node diodes
  - Bridging attaches a higher layer intermediary
  - Add a piece of drainage diffusion to leak away charge



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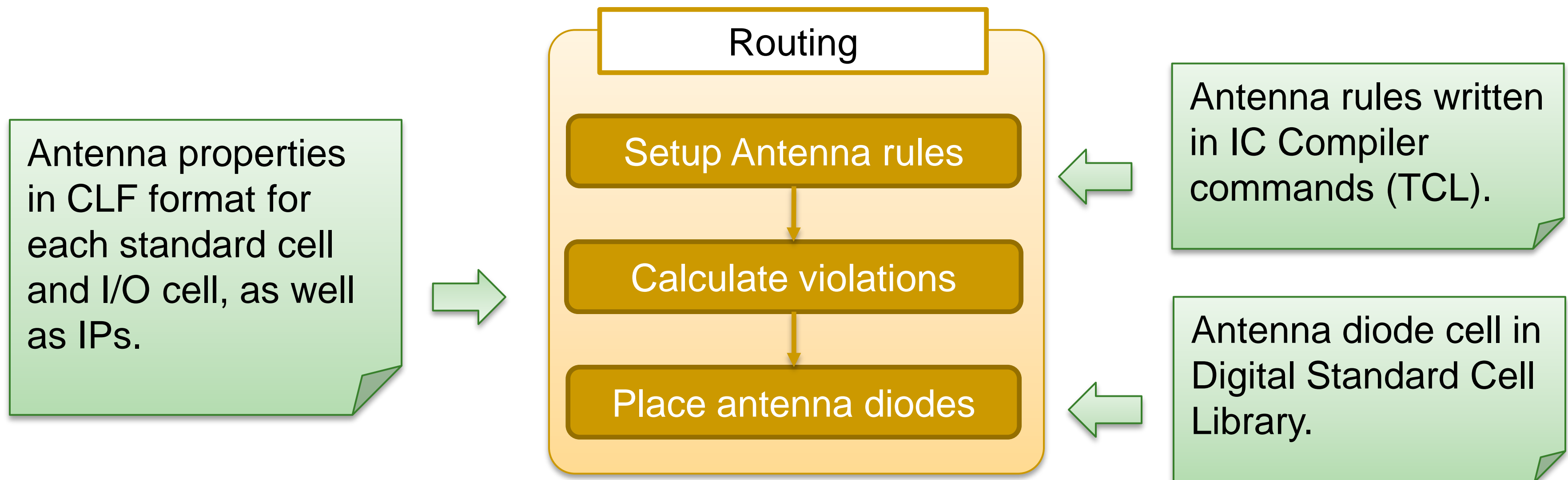
Antenna Fixing: Flow and Required Data

- Contemporary automated physical synthesis tools (IC Compiler, for example) are able to automatically fix antenna violations
- Additional technology and library data should be provided



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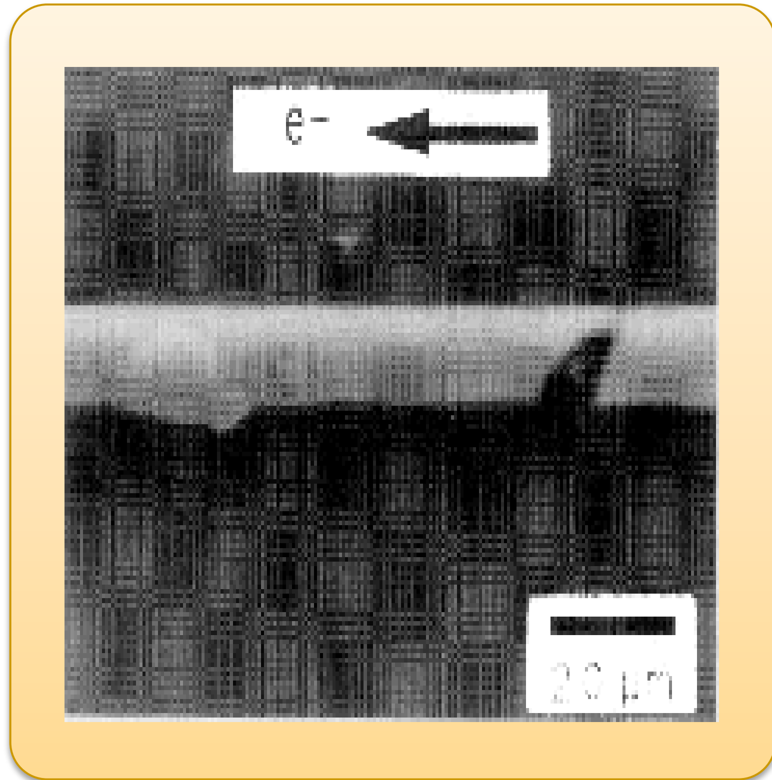
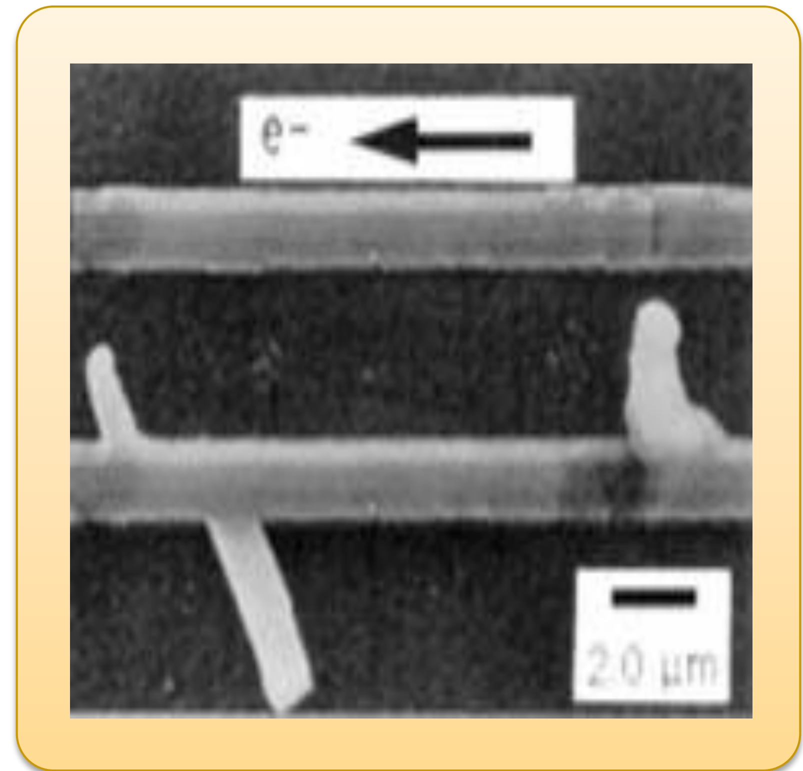
Electromigration Effects

Metal void -> open circuit

Metal hillock -> short circuit





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Electromigration Rules

- Current density
  - Electromigration is not a function of current, but a function of current density
  - Larger current on narrower metal width or smaller via area speeds up electromigration effect
- Temperature
  - Electromigration is accelerated by elevated temperature

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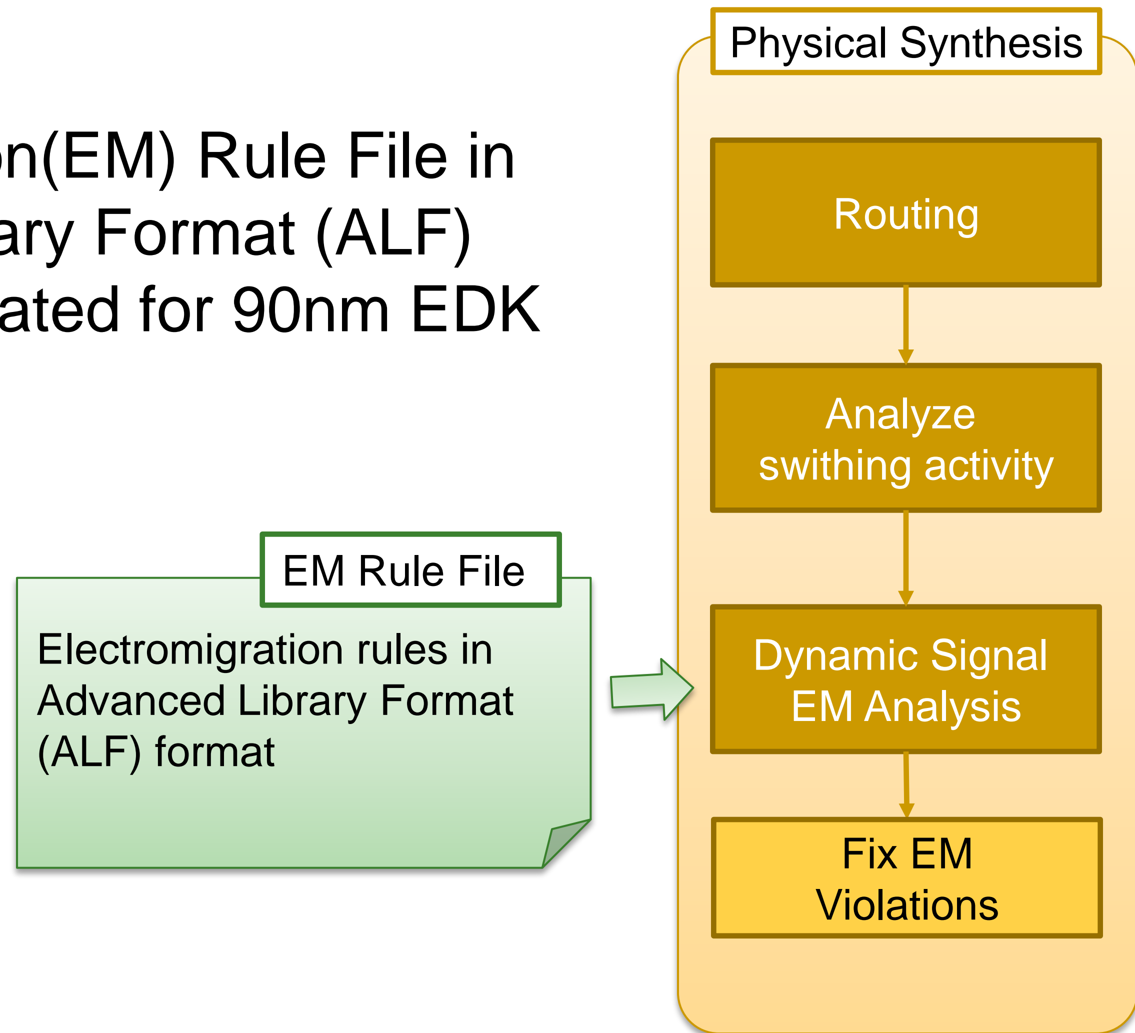
Electromigration Fixing

- Electromigration(EM) Rule File in Advanced Library Format (ALF) format was created for 90nm EDK



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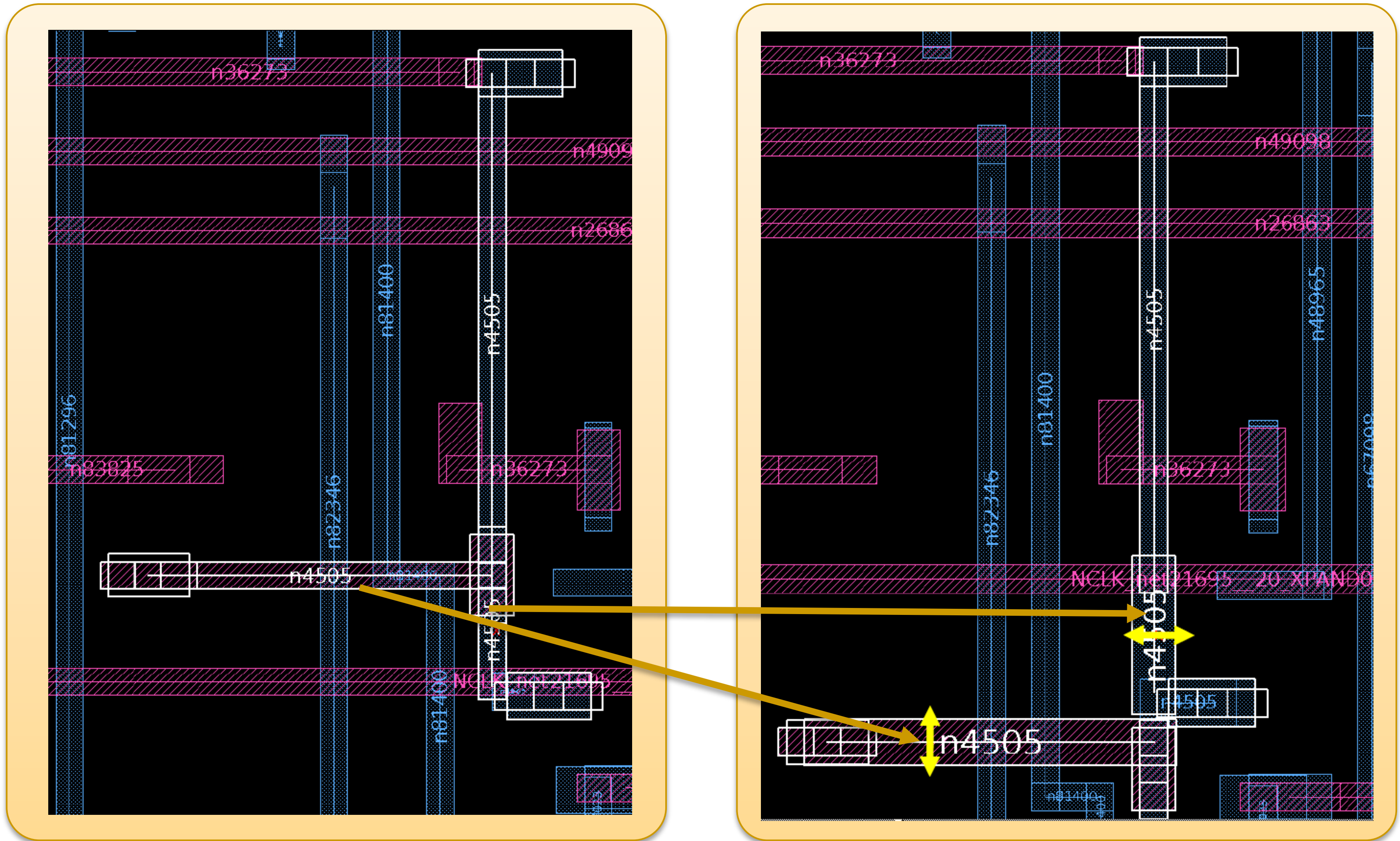
Electromigration Fixing Results



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SAED 90nm Educational Design Kit (EDK)

90nm EDK Content

Digital Standard Cell Library

- **340 cells**, operating at **300 MHz**.
- **Special cells** for low power design.
- **Standard, Low** and **High V_{th}** versions

I/O Standard Cell Library

- **50** typical I/O cells, 1.2V/2.5V operation, **Wire-bond** and **Flip-Chip** versions.

I/O Special Cell Library

- **SSTL, HSTL, PCI** cells. Implemented according to standards.

Set of Memories

- **35 static RAMs (SRAMs).**
  Dual and single port SRAMs with the same architecture and different size.

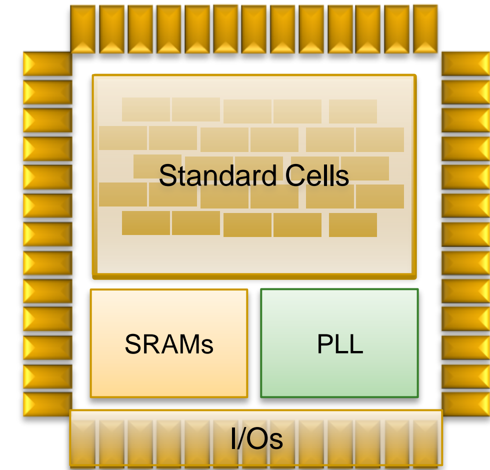
Phase Locked Loop

- **3 operating modes**: normal, external feedback and bypass.

References to different designs

- **OpenSPARC T1, PowerPC 405, Leon3, ChipTop, Orca.**

Contains



Supports

- Modern Low Power design
- Wire-bond/Flip-chip I/O
- I/O standards (PCI, etc.)
- OpenSPARC T1 processor

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90nm EDK: Technology Kit

Technology Kit

Documentation

Design Rules	Layer Map	Device Formation	Process Description

Technology

Spice models	Technology file	Pcells	Electro-migration	Antenna

Verification/Extraction

- Hercules/IC Validator
  - DRC
  - LVS
  - Density
  - Fill Utility
- StarRC
  - ITF
  - Fill Estimation
  - TLU+
  - GRD

Scripts, supporting design flow

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90nm EDK: Digital Standard Cell Library

Digital Standard Cell Library (DSCL)

- Aimed at optimizing the main characteristics of designed Ics
- Contains 340 cells, cell list compiled based on the requirements for educational designs
- Typical combinational and sequential logic cells for different drive strengths

Typical combinational and sequential

- Inverters/Buffers
- Logic Gates
- Flip-Flops (regular+scan)
- Latches
- Delay Lines
- Physical (Antenna diode)

Special cells for different styles LPD

- Isolation Cells
- Level Shifters
- Retention Flip-Flops
- Clock gating
- Always-on Buffers
- Power Gating

- Provides the support of IC design with different core voltages to minimize dynamic and leakage power.

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Operating Conditions and Drive Strengths

Operating conditions

Parameter	Min	Typ	Max	Units
Power Supply (VDD) range	0.7	1.2	1.32	V
Operating Temperature range	-40	+25	+125	°C
Operating Frequency (F)	-	300	-	MHz

Drive strengths

Drive Strength	Cell Load
X0	0.5x C_{sl}
X1	1x C_{sl}
X2	2x C_{sl}
X3	3x C_{sl}
X4	4x C_{sl}

Drive Strength	Cell Load
X8	8x C_{sl}
X12	12x C_{sl}
X16	16x C_{sl}
X24	24x C_{sl}
X32	32x C_{sl}

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Characterization Corners

Corner Name	Process (NMOS proc. – PMOS proc.)	Temperature (T)	Power Supply (V)	Notes
TTNT1p20v	Typical - Typical	25	1.2	Typical corner
SSHT1p08v	Slow - Slow	125	1.08	Slow corner
FFLT1p32v	Fast - Fast	-40	1.32	Fast corner
FFHT1p32v	Fast - Fast	125	1.32	High leakage corner
SSLT1p32v	Slow - Slow	-40	1.32	Low temperature corners
SSLT1p08v	Slow - Slow	-40	1.08	
Low Voltage Operating Conditions				
TTNT0p80v	Typical - Typical	25	0.80	Typical corner
SSHT0p70v	Slow - Slow	125	0.70	Slow corner
FFLT0p90v	Fast - Fast	-40	0.90	Fast corner
FFHT0p90v	Fast - Fast	125	0.90	High leakage corner
SSLT0p90v	Slow - Slow	-40	0.90	Low temperature corners
SSLT0p70v	Slow - Slow	-40	0.70	

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90nm EDK: I/O Cell Library

I/O Standard Cell Library (IOSCL)

- Uses 90nm EDK 1P9M 1.2V/2.5V design rules
- Includes typical I/O cells which are necessary for IC design
- Cell list compiled based on the analysis of different educational designs
- Contains 50 cells

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90nm EDK: Phase Locked Loop

Phase Locked Loop (PLL)

- Uses 90nm EDK 1P9M 1.2V/2.5V process
- Is clock multiplier circuit
- Has 3 operating modes
  - normal
  - external feedback
  - bypass
- Has 3 frequency modes
  - 30 MHz
  - 60 MHz
  - 120 MHz

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90nm EDK: Set of Memories

Set of Memories

35 static RAMs (SRAMs)

Synchronous SRAMs

Dual-Port | Single port

Same architecture different width x depth

Contains also 21 OpenSPARC T1 cache cells

Word (bit)	Words	Cell Name
4	16	SRAM4x16
	32	SRAM4x32
	64	SRAM4x64
	128	SRAM4x128
8	16	SRAM8x16
	32	SRAM8x32
	64	SRAM8x64
	128	SRAM8x128
16	16	SRAM16x16
	32	SRAM16x32
	64	SRAM16x64
	128	SRAM16x128
32	16	SRAM32x16
	32	SRAM32x32
	64	SRAM32x64
	128	SRAM32x128
	…	

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Deliverables

N	Type	Description
1	.doc, pdf	Databook / User guide
3	.db, .lib	Logic Models
4	.v	Verilog simulation/power models
5	.vhd	VHDL / Vital simulation models
6	.cdl, .sp	LVS, HSPICE netlists
7	.spi	Extracted C or/and RC netlists for different corners
8	.gds	GDSII layout views
9	.lef	LEF files
10	.FRAM, .CEL	Fram views, layout views and runset files
11	.clf	Antenna data

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Conclusion

- Technological progress causes many IC Design challenges
- For number of challenges solutions were implemented in SAED 90nm EDK
- SAED 90nm EDK together with Synopsys EDA tools make it possible to develop complex designs while addressing these challenges

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