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Low Power Design Methods: Design Flows and Kits

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Low power design flows

Power-Aware Design Flow

Deep submicron technology, from 130nm on, poses a new set of design problems. We can now implement tens of millions of gates on a reasonably small die, leading to a power density and total power dissipation that is at the limits of what packaging, cooling, and other infrastructure can support. As technology has shrunk to 90nm and below, the leakage current is increasing dramatically, to the point where, in some 65nm designs, leakage current is nearly as large as dynamic current. This power density not only presents packaging and cooling challenges; it also can pose problems for reliability, since the mean time to failure decreases exponentially with temperature. In addition, timing degrades with temperature and leakage increases with temperature. To combat these problems, designers are using aggressive approaches at every step of design process from software to implementation. These approaches include power gating, where blocks are powered down when not in use, and multi-threshold libraries that can trade-off leakage current for speed. So, power management challenges need to be taken into account starting from early stages of design, and every other step should consider power management from the viewpoint of that design level. To comply with modern low power design (LPD) techniques, conventional design flows are modified to handle power-aware design at every step.

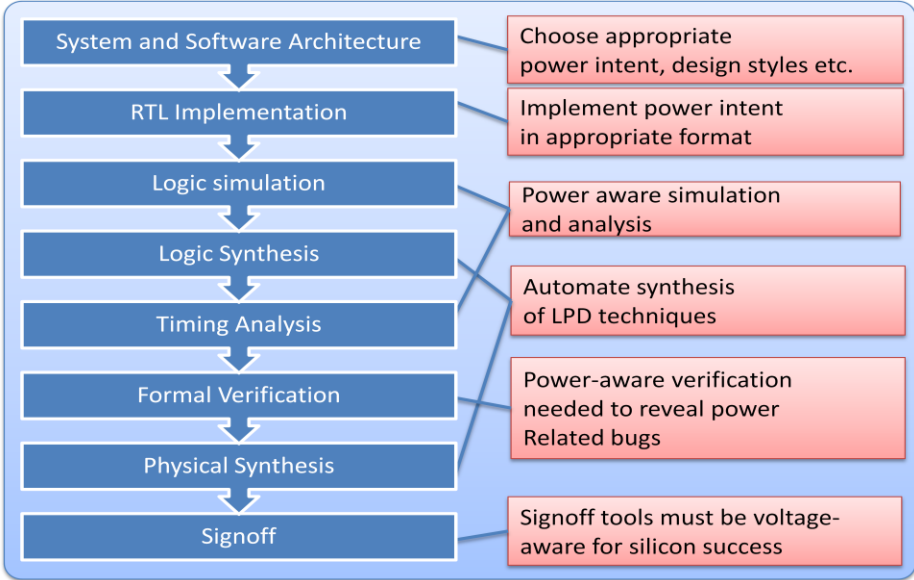


Figure 1 Power aware design flow

On the system level appropriate power intent should be chosen according to the peculiarities of the design. For example on the early stages of the design it is already known which parts should operate at maximum performance and which could be shut down during some periods of time. Then, during RTL implementation stage, power intent also should be implemented, this could be done directly in RTL, but this is now not used, there are special languages or formats which help designers to specify power management. We will discuss it later. Also designers should have power aware logic simulation tools to be able to test their intent on early stages of design.

Another large modification to design flow is that logic and physical synthesis tools need to be modified to be able to implement LPD techniques automatically. Formal verification tool are also modified to be able to check gate level design against initial RTL and power intent. The last stage, signoff, also should be modified as having different voltages, on the same design raises challenges that need to be taken into account in order for silicon success.

Though we already know the general design flow is modified to comply with LPD techniques, different techniques are treated differently by design implementation tools and require different effort level depending on their complexity. Clock Gating and Multi-Threshold LPD techniques usually require less efforts, as modern tools are able to automatically perform such optimizations. In contrast, Multi Voltage and Power Gating techniques require providing architectural level power management strategy as an input to tools. Thus, these 2 techniques require more design flow modifications with regards to additional data that is given to the flow with the help of Unified Power Format (UPF).

Unified Power Format (UPF)

The necessary changes of the conventional design flows require tools to be able to automate power-aware design. Contemporary automated design tools are designed around hardware description languages which are used for behavioral description of designs which later used as input to synthesis tools. The complexity in using LPD techniques comes from the fact that we need to define virtual logical/physical power structures. No existing HDL or system-level constructs could reliably support the specification of power management and power distribution. Further, vendor-specific formats are non-portable and are closed so they can't be distributed or used with other vendor tools.

As HDL languages have no power constructs and scripting languages are mostly vendor specific a new comprehensive and interoperable solution was demanded by the industry. Unified power format (UPF) provides this functionality. UPF describes low power intent for design implementation, analysis and verification. It enables open, multi-vendor tool flows and solutions for low-power ASIC and SoC design.

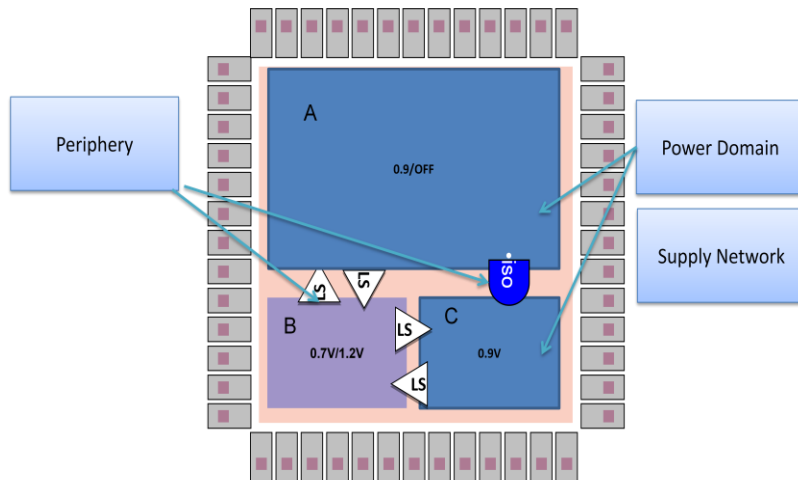


Figure 2 Power intent specification

To specify the power intent, the following information must be given to the implementation tool: the groups of logic hierarchies that share the same power characteristics, including power net requirements, power switching styles and power down control signals, if any, must be specified. Such groups are called power domains. For these groups their supply voltages, ports and supply connections, in other words, information about their supply network should also be provided. Between different power domains special cells, such as level shifters, isolation cells, always-on buffers should be placed. These cells should be specified so that the tools will automatically insert them during the synthesis steps. And finally, as the power states of all these blocks are in relationships, it is very important to provide a synthesis tool with comprehensive information about all legal power states of these blocks including the powering sequence for the blocks. So, for a LPD design, the power intent must be taken into account throughout the entire design flow, from RTL to Physical implementation.

Power-Aware Design Flow Modification with UPF

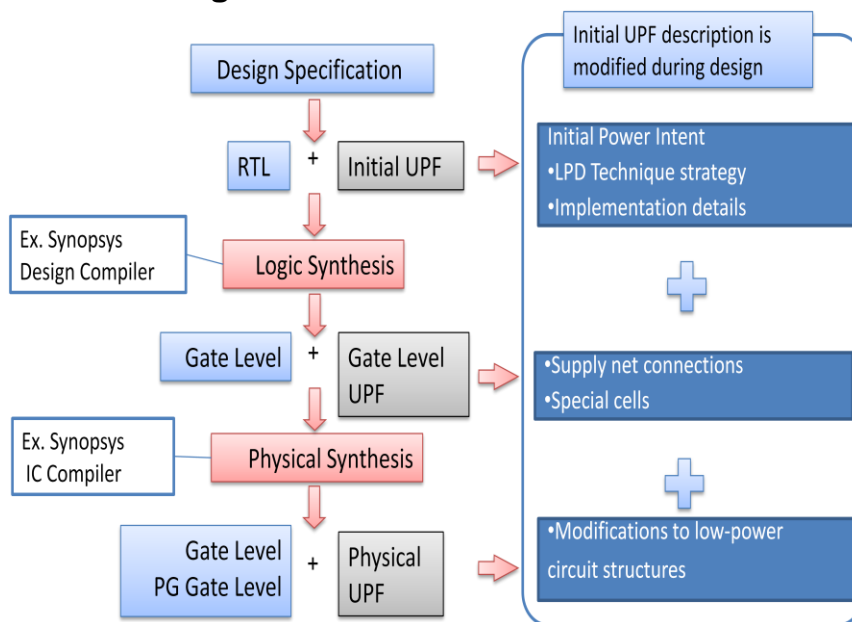


Figure 3 Design flow modification with UPF

A robust UPF-compliant “power aware” flow starts with the register-transfer level (RTL) description of the logic of the design, together with a UPF file. The initial UPF file can be developed collaboratively among system engineers, RTL designers, and physical designers. The RTL and UPF descriptions are contained in separate files so that they can be maintained and modified separately.

The logic synthesis step (Synopsys Design Compiler is used) produces a gate-level netlist and an updated UPF file. This gate-level UPF file contains the RTL UPF information plus explicit supply net connections for special cells created during synthesis. The physical synthesis tool (Synopsys IC Compiler is used) reads in the gate-level netlist and gate-level UPF and performs physical implementation (placement and routing), producing an optimized gate-level netlist, a complete power and ground (PG) netlist, and an updated UPF file. This UPF file contains previous UPF information plus any modifications to low-power circuit structures resulting from physical implementation, such as power switches.

Library Requirements for LPD

Besides impact of LPD techniques on design flows, they impact digital standard cell libraries as well. In order to meet LPD requirements, Digital Standard Cell Libraries must also be enhanced. They must include special cells, for example level shifters to handle multi-voltage designs, or versions of cells with different threshold voltages for multi-threshold designs. Low Power designs require new cells with multiple power pins to define multiple power ground pin information accurately. All these requirements will be discussed on the example of SAED90nm Digital Standard Cell Library (DSCL) which was developed

at Synopsys Armenia Educational Department (SAED). The Digital Standard Cell Library developed at SAED has been built using 90nm EDK 1P9M 1.2V/2.5V design rules. The library has been created aimed at optimizing the main characteristics of designed ICs by its help. The library includes typical miscellaneous combinational and sequential logic cells for different drive strengths. Besides, the library contains all the cells which are required for different styles of low power (multi-voltage, multi threshold) designs. Those includes: Level Shifters, Isolation Cells, Retention Flip-Flops and others. The presence of all these cells provides the support of IC design with different core voltages to minimize dynamic and leakage power. Cell list compiled on the basis of analysis of different educational designs, contains all cells needed for educational purposes. Digital Standard Cell library contains 340 cells.

Special Cells for LPD

The first special cell that is used in LPD techniques is Level-shifter. When driving signals between power domains with radically different power rails, level shifters are needed to shift a signal that comes in at one voltage level to an output that is at a different voltage level. Level shifters do not affect the functionality of the design; from a logical perspective they are just buffers. For this reason, modern implementation tools can automatically insert level shifters where they are needed. No change to the RTL is required. Typically level shifters are placed in the receiving domain – in the lower domain for High-to- Low shifters, in the higher domain for High-to-Low shifters.

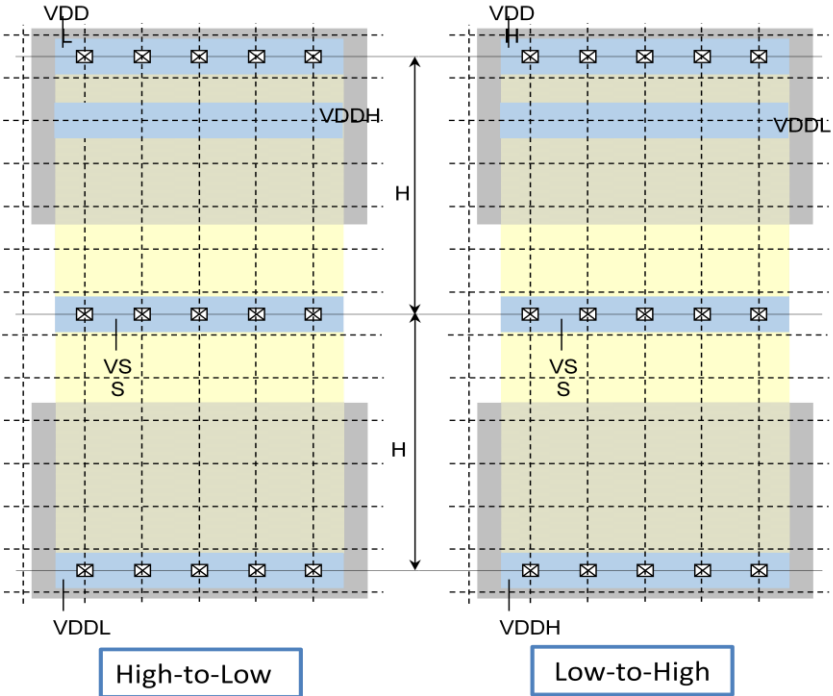


Figure 4 Physical structure of the Level-shifter

Typically level converters are double height cells with two supply rails and a common ground. From the physical structure perspective, the main differences in the physical structures between this

special cell and standard cells are the double height and 2 power rails. Level shifters in SAED90nm DSCL were designed with respect to this requirement.

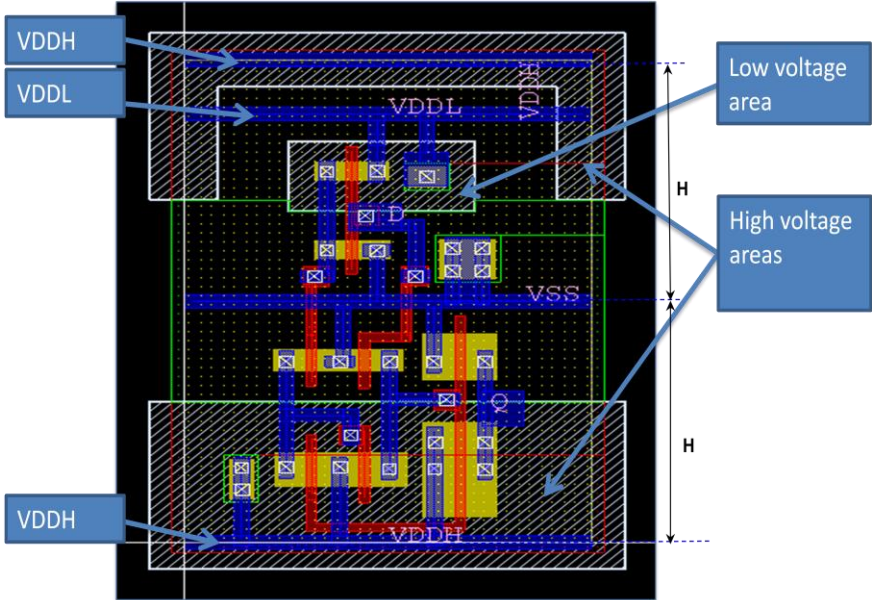


Figure 5 SAED90nm DSCL Level shifter layout

For implementation of Power gating LPD technique, when selectively powering down certain blocks in the chip while keeping other blocks powered up. The goal of power gating is to minimize leakage current by temporarily switching power off to blocks that are not required in the current operating mode. One challenge for power gating designs is that the outputs of the power gated block may ramp off very slowly. The result could be that these outputs spend a significant amount of time at threshold voltage, causing large crowbar currents in the always powered on block. To prevent these crowbar currents, isolation cells are placed between the outputs of the power gated block and the inputs of the always on block. The layout of Isolation cell from SAED90nm DSCL is illustrated.

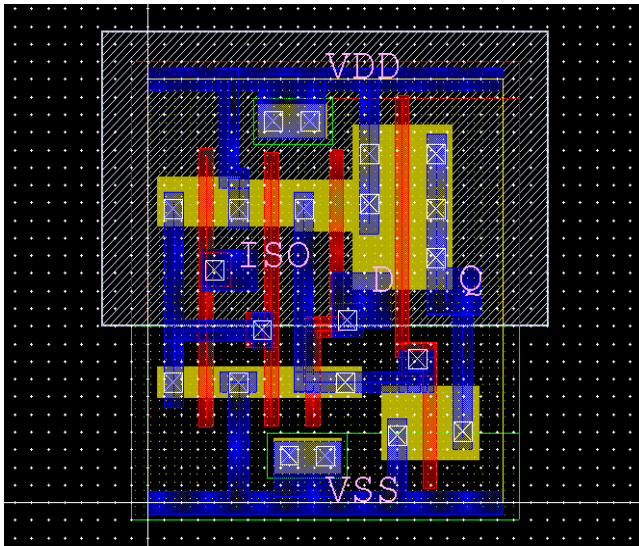


Figure 6 SAED90nm DSCL Isolation cell layout

When dealing with shut-down partitions, there can be some situations in which certain cells in the shut-down partition need to continuously stay active. For this purpose always-on cells are used. The basic difference between an always-on cell and a regular cell is that the always-on cell has an extra power supply that serves as back-up during shut-down mode. In these always-on cells the switchable VDD and/or VSS buses can float. The always-on VDD/VSS in such cells can be considered as an additional input. During the routing stage of digital design these inputs are connected to unswitched power/ground.

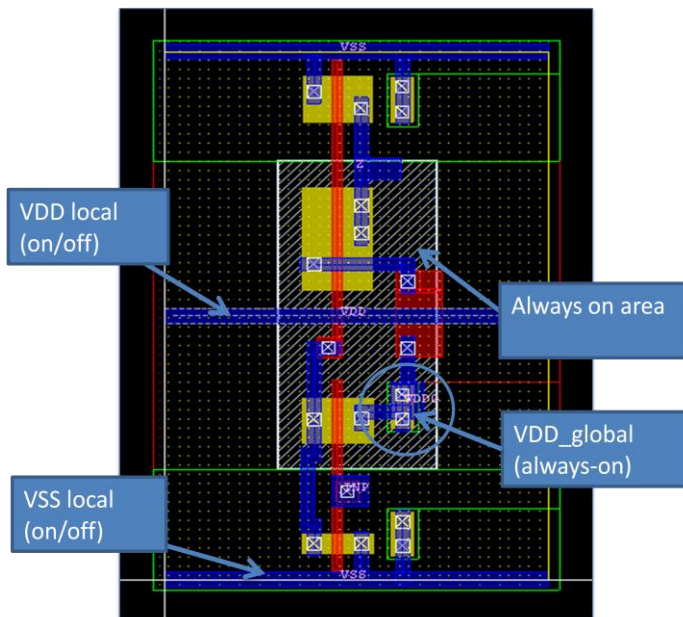


Figure 7 SAED90nm DSCL Always-on buffer layout

In cases when ISO cells are to be placed in power switched areas they have to be supplied from global (non-switchable) supply. It is necessary to isolate the outputs of a power gated block in order to

avoid the electrical problem of floating outputs driving inputs of powered-up blocks. Logically, it makes no difference whether we clamp these signals at their source – that is, inside the power gated block – or at their destination – that is, in the powered-up blocks. But there are important practical considerations that affect this choice. It is likely that at least some of the outputs of the power gated block go to more than one powered-up block. If the outputs are isolated at the receiving blocks, more than one isolation cell may be required for each output. Therefore it is more area-efficient to isolate the outputs inside the power gated block. Isolating outputs at their source does present some constraints for place and route, however. Unlike the other gates in the power gated block, the isolation cells must remain powered during power-down. Thus, the power domain containing the power gated block must now provide both switched power and always-on power. This somewhat complicates power routing of the chip, but modern EDA tools are capable of solving this problem. The only difference between isolation and always-on isolation cells is the secondary always-on power rail.

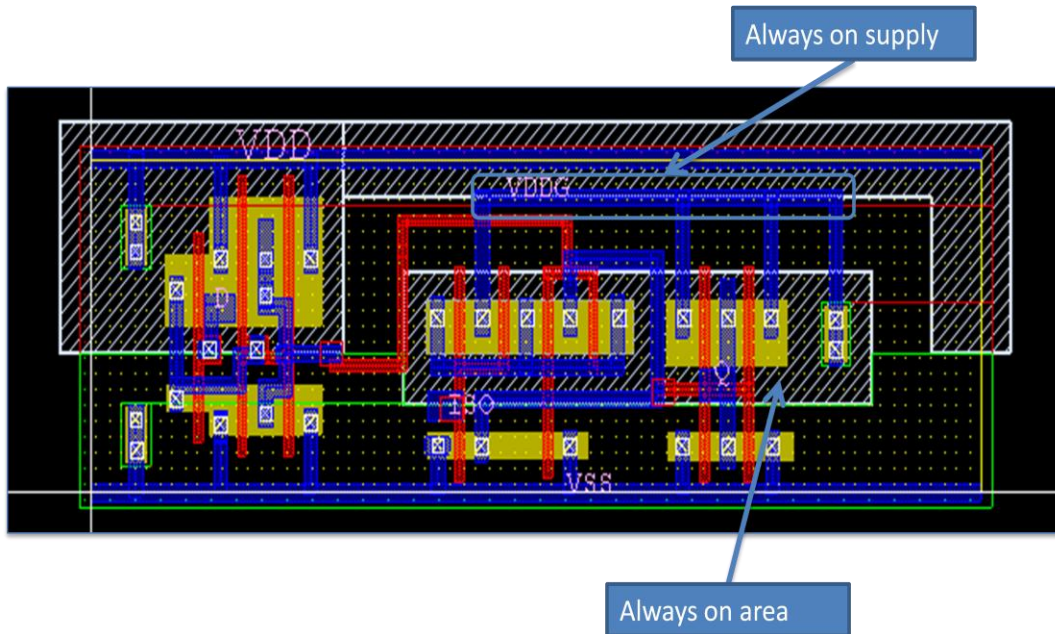


Figure 8 SAED90nm DSCL Always-on Isolation cell layout

When a partition is shut down and later powered-up again, it is often necessary for the partition to resume operation based in its last good state. Such a retention strategy can save significant amounts of time and power during power up. One commonly used design technique to implement this, is to use special registers which can store the state during shutdown mode. These special registers are referred to as state-retention registers or simply retention registers. Retention registers typically have an auxiliary or shadow register that is slower than the main register but which has much less leakage current. The shadow register is always powered up, and stores the contents of the main register during power gating. These retention registers need to be told when to store the current contents of the main register into the shadow register and when to restore the value back to the main register. This control is provided by the power gating controller. The most common approach to provide state retention during power gating is to replace a standard register with a retention register. These retention registers ensure

that once the block is awake, after being asleep, the state of the block can be restored within a few cycles. This method trades off area and leakage for reduced time being required to bring the “sleeping” block to a known, useful state. Other methods, like scanning out the state to memory, or completely resetting the block, allow for slightly lower leakage but typically take many cycles to return the previously shut down logic to a known, useful state. Those methods also will use more dynamic power than state retention registers to bring the logic to the same useful state because of the number of cycles required. When considering state retention register usage at the floorplanning stage, the secondary or backup supply connections to the retention registers have to be considered also, so that there will not be IR-drop or EM issues on the backup supply mesh.

The layout of SAED90nm DSCL Retention register is illustrated. In the always-on area transistors are high-voltage and are slower than the main register transistors but have much less leakage current.

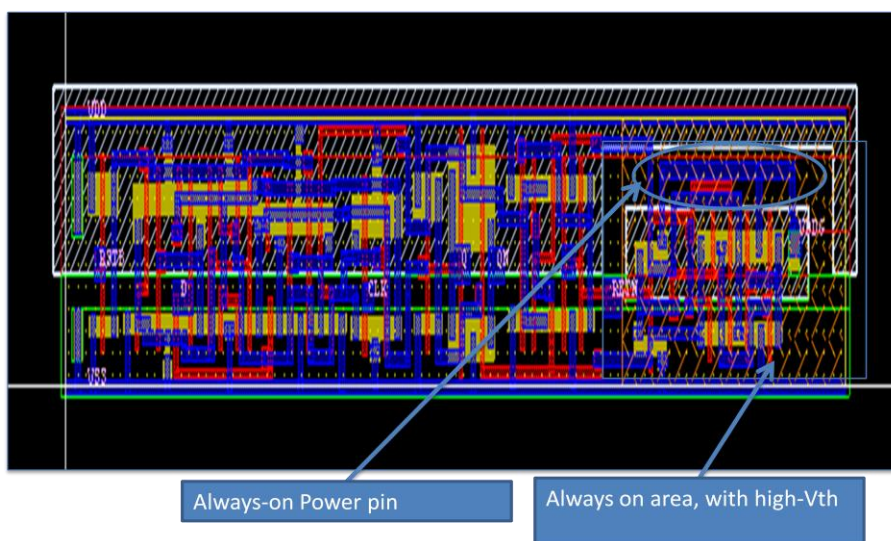


Figure 9 SAED90nm DSCL Retention register layout

Multi-Threshold Libraries

In contrast to techniques like clock-gating and multi-voltage design that need special cells, multi-threshold design synthesis requires presence of multi-Vth libraries. As a rule, they contain three variants for the same digital standard cell – low Vth, standard Vth and high Vth. Usually all three variants of the same cell have the same name in the library and a modifier specifying the threshold type. This approach will enable to lower leakage by using leaky low VT transistors only on critical timing paths. The implementation tools can take advantage of these libraries to optimize timing and power simultaneously. The goal of this approach is to minimize the total number of fast, leaky low VT transistors by deploying them only when required to meet timing. As the SAED90nm DSCL was developed to handle LPD techniques, it contains 3 variants of all 340 cells: the same cell is available with low Vth, standard Vth and high Vth.

Additional characterization corners

In order to fully meet the requirements of low power design techniques, SAED90nm DSCL was characterized for the 16 process/voltage/temperature conditions shown in table. Composite Current Source (CCS) modeling technology was used for cell characterization to meet the requirements of contemporary low power design methods. CCS provides timing, noise, and power analyses while considering the relevant nanometer dependencies. Also some additional corners were used to characterize level shifters - both low-to-high and high-to-low. There are 12 corners for each type.

Additional data

Along with all the requirements already discussed, Low power DSCLs must also include PG pin definitions for all cells. This will let the implementation tools to perform power domain driven synthesis, automatically connect power nets and etc. SAED90nm DSCL also contains Power verilog models. These are separate verilog models where output is modeled depending on power.

In summary, SAED90nm DSCL was developed to handle low power designs, so it includes all necessary special cells for such designs.

Conclusion

In conclusion, it must be mentioned that Low power design techniques require significant design flow modifications. They also have their huge impact on digital standard cell libraries. DSCL of SAED90nm Educational Design Kit (EDK) was created to meet these requirements. It includes all special cells needed for low power design techniques and is currently in use in 235 universities of 37 countries. All this universities are involved in Synopsys worldwide university program. Also the EDK is used Inside Synopsys for education of customers low power design techniques.