Low Power Design Methods: Design Flows and Kits

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March 23, 2011
Outline

• Low Power Design Flows
• Library requirements for Low Power Design
• Example of 90nm EDK
Conventional Design Flow

Almost every step of design flow need to be modified for LPD

System and Software Architecture

RTL Implementation

Logic simulation

Logic Synthesis

Timing Analysis

Formal Verification

Physical Synthesis

Signoff

Power Management should be taken into account at the earliest design stages
Power-Aware Design Flow

- System and Software Architecture
  - Choose appropriate power intent, design styles etc.

- RTL Implementation
  - Implement power intent in appropriate format

- Logic simulation

- Logic Synthesis
  - Power aware simulation and analysis

- Timing Analysis
  - Automate synthesis of LPD techniques

- Formal Verification
  - Power-aware verification needed to reveal power Related bugs

- Physical Synthesis

- Signoff
  - Signoff tools must be voltage-aware for silicon success
LPD Techniques Automation Levels

Clock Gating

Multi-threshold

Automatically

No special treatment needed

Power gating

Multi Voltage

Automatically

Specification of power intent (UPF)

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# Unified Power Format (UPF): Necessity

<table>
<thead>
<tr>
<th>Language</th>
<th>Specification of power intent</th>
<th>Interoperable among EDA tools</th>
<th>Can be freely used (open standard)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Hardware Description Languages (Verilog, VHDL, etc.)</td>
<td>-</td>
<td>+</td>
<td>+</td>
</tr>
<tr>
<td>Vendor –Specific Formats</td>
<td>+</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>UPF</td>
<td>+</td>
<td>+</td>
<td>+</td>
</tr>
</tbody>
</table>
Specifying Power Intent

Operation Scenario
(OFF, 0.9V, 0.7V)
(0.9V, 0.9V, 1.2V)

MV with power gating
MV with Power Gating Example
UPF: Power Domains

<table>
<thead>
<tr>
<th>Power Domain</th>
<th>Power State</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>0.9/OFF</td>
</tr>
<tr>
<td>B</td>
<td>0.7/1.2</td>
</tr>
<tr>
<td>C</td>
<td>0.9</td>
</tr>
</tbody>
</table>
UPF: Supply Network

**UPF**

<table>
<thead>
<tr>
<th>Supply Net</th>
<th>Voltage Level (V)</th>
<th>Power Domain</th>
</tr>
</thead>
<tbody>
<tr>
<td>VDD</td>
<td>0.9</td>
<td>C</td>
</tr>
<tr>
<td>VDDA</td>
<td>0.7</td>
<td>B</td>
</tr>
<tr>
<td>VDDB</td>
<td>1.2</td>
<td>B</td>
</tr>
<tr>
<td>VDDV</td>
<td>Virtual 0.9</td>
<td>A</td>
</tr>
<tr>
<td>VSS</td>
<td>Common Ground</td>
<td>A/B/C</td>
</tr>
</tbody>
</table>
UPF: Periphery

Required Periphery

- Level Shifters between A and B
- Level Shifters between B and C
- Isolation between C and A
- Retention Cell inside A
- Control Block inside A
UPF: State Scenario

<table>
<thead>
<tr>
<th>Scenario</th>
<th>A</th>
<th>B</th>
<th>C</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.9/0.7/0.9</td>
<td>Allowed</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0.9/1.2/0.9</td>
<td>Allowed</td>
<td></td>
<td></td>
</tr>
<tr>
<td>OFF/0.7/0.9</td>
<td>Allowed</td>
<td></td>
<td></td>
</tr>
<tr>
<td>OFF/1.2/0.9</td>
<td>Not Allowed</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Design Flow Modification with UPF

Design Specification

RTL + Initial UPF

Logic Synthesis

Gate Level + Gate Level UPF

Physical Synthesis

Gate Level PG Gate Level + Physical UPF

Initial Power Intent
- LPD Technique strategy
- Implementation details

Ex. Synopsys Design Compiler

Ex. Synopsys IC Compiler

Initial UPF description is modified during design

• Supply net connections
• Special cells

• Modifications to low-power circuit structures
Design Compiler Visual UPF

Strategies Visualization

- Supply port
- Block PD primary power net
- Retention register
- Top PD primary ground net
- PD boundary
- Power Switch
- ISO location parent with backup power defined
- LS strategy defined in UPF

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IC Compiler UPF Placement

- Placement respects voltage area boundary
- Special Level Shifter and Isolation Cells placement
  - Special cells placed closer to VA boundary
Library Requirements for LPD

- Special cells
- Special versions of library
- Characterization in additional corners
- Additional views/files/attributes
90nm EDK: Digital Standard Cell Library

Aimed at optimizing the main characteristics of designed ICs.

Contains 340 cells, cell list compiled based on the requirements for educational designs.

Typical combinational and sequential logic cells for different drive strengths.

Typical combinational and sequential:
- Inverters/Buffers
- Logic Gates
- Flip-Flops (regular+scan)
- Latches
- Delay Lines
- Physical (Antenna diode)

Special cells for different styles LPD:
- Isolation Cells
- Level Shifters
- Retention Flip-Flops
- Clock gating
- Always-on Buffers
- Power Gating

Provides the support of IC design with different core voltages to minimize dynamic and leakage power.
Special Cells for LPD: Level Shifter

Level Shifters
Level Shifter

Logic Symbol of Low to High Level Shifter

Low to High Level Shifter Truth Table

<table>
<thead>
<tr>
<th>D (0.8V)</th>
<th>Q (1.2V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

Logic Symbol of High to Low Level Shifter

High to Low Level Shifter Truth Table

<table>
<thead>
<tr>
<th>D (1.2V)</th>
<th>Q (0.8V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>
Level Shifter Physical Structure

High-to-Low

Low-to-High
Level Shifter (High to Low) Physical Design

High voltage areas

Low voltage area

VDDH

VDDL
Level Shifter (Low to High) Physical Design

VDDH
VDDL

Low voltage area
High voltage areas

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Special Cells for LPD: Isolation Cells

Power Gating

Isolation Cells

OFF/0.7
Isolation Cells

Logic Symbol of Clamp 0
Isolation Cell (Logic AND)

Logic Symbol of Clamp 1
Isolation Cell (Logic OR)

Hold 0 Isolation Cell (Logic AND) Truth Table

<table>
<thead>
<tr>
<th>D</th>
<th>ISO</th>
<th>Q</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>X</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

Output clamped

Hold 1 Isolation Cell (Logic OR) Truth Table

<table>
<thead>
<tr>
<th>D</th>
<th>ISO</th>
<th>Q</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>X</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

Bypass mode

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Special Cells for LPD: Always-on Buffers

Power Gating

Always on cells

0.9

0.7 – 1.08

OFF/0.7
Always-on Buffer

Logic Symbol of Always on Non-Inverting Buffer

Always on Non-Inverting Buffer Truth Table

<table>
<thead>
<tr>
<th>IN</th>
<th>VDDG</th>
<th>VSS</th>
<th>Q</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>
Special Cells for LPD: Always-on Isolation cells
Always on Isolation Cells

Hold 0 Isolation Cell (Logic AND) Truth Table

<table>
<thead>
<tr>
<th>D</th>
<th>ISO</th>
<th>Q</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>X</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

Hold 1 Isolation Cell (Logic OR) Truth Table

<table>
<thead>
<tr>
<th>D</th>
<th>ISO</th>
<th>Q</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>X</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

Logic Symbol of Clamp 0 Isolation Cell (Logic AND), Always On

Logic Symbol of Clamp 1 Isolation Cell (Logic OR), Always On

Output clamped

Bypass mode
Isolation Cell (always-on) Physical Design

Always on area

Always on supply
Special Cells for LPD: Enable level shifters

- Combination of Level Shifter and ISO cell
Level Shifters With Active Low Enable

Symbol of Low to High Level Shifter
Active Low Enable, Clamp 0

Symbol of High to Low Level Shifter
Active Low Enable, Clamp 1

<table>
<thead>
<tr>
<th>D(0.8V)</th>
<th>ENB</th>
<th>Q(1.2V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>X</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

Bypass mode

<table>
<thead>
<tr>
<th>D(1.2V)</th>
<th>ENB</th>
<th>Q(0.8V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>X</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

Bypass mode

Output clamped
Enable Level Shifter (low-to-high)
Physical design

VDDH
VDDL

Low voltage area
High voltage areas
State Retention Registers

- Retention Register - preserve status while the logic is turned off.

1.08V/OFF
0.7V
CTR
0.9V

State Retention Registers
Retention Register Physical design

Always-on Power pin

Always on area, with high-Vth
Power Gates

- Retention Register - preserve status while the logic is turned off
- Coarse Grain - Power Gates (switch cells)
Header Cells

Logic Symbol of Header Cell

Header Cell Truth Table

<table>
<thead>
<tr>
<th>SLEEP</th>
<th>VDDG</th>
<th>VDD</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>hi-z</td>
</tr>
</tbody>
</table>

Logic Symbol of Header Cell (with SLEEPOUT output)

Header Cell (with SLEEPOUT output) Truth Table

<table>
<thead>
<tr>
<th>SLEEP</th>
<th>VDDG</th>
<th>VDD</th>
<th>SLEEPOUT</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>hi-z</td>
<td>1</td>
</tr>
</tbody>
</table>
Header Cells Physical Design

a. Header Cell

b. Header Cell (with SLEEPOUT output)
Multi-Threshold Libraries

![Diagram of logic gates and critical path]

- Multi-V\textsubscript{th} libraries
  - AL
  - BL
  - CL
  - AS
  - BS
  - CS
  - AH
  - BH
  - CH
  - Low Vth
  - Std Vth
  - High Vth

![Graph showing leakage and delay across Low-V\textsubscript{th}, Std-V\textsubscript{th}, High-V\textsubscript{th}]

- Critical Path

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DSCL: Multi Threshold Versions of Cells

• For implementation of Multi-Vth technique the whole DSCL is available in 3 versions (1020 cells)
  ▪ All cells with Low– threshold voltage
  ▪ All cells with Standard – threshold voltage
  ▪ All cells with High– threshold voltage
Characterization

- Characterization computes cell parameter (e.g. delay, output current) depending on input variables: output load, input slew, etc.
- Characterization is performed for various combinations of operating conditions: process, voltage, temperature (also called PVT corners).

Input Slew

![Diagram of input slew and output current](image)

Characterization processes:
- **Process: Typical**
  - Temp: 25°C
  - Voltage: 1.2V

- **Process: Slow**
  - Temp: -40°C
  - Voltage: 1.08V

- **Process: Fast**
  - Temp: 125°C
  - Voltage: 1.32V
## DSCL: Characterization Corners

<table>
<thead>
<tr>
<th>Corner Name</th>
<th>Process (NMOS proc. – PMOS proc.)</th>
<th>Temperature (T)</th>
<th>Power Supply (V)</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>TTNT1p20v</td>
<td>Typical - Typical</td>
<td>25</td>
<td>1.2</td>
<td>Typical corner</td>
</tr>
<tr>
<td>SSHT1p08v</td>
<td>Slow - Slow</td>
<td>125</td>
<td>1.08</td>
<td>Slow corner</td>
</tr>
<tr>
<td>FFLT1p32v</td>
<td>Fast - Fast</td>
<td>-40</td>
<td>1.32</td>
<td>Fast corner</td>
</tr>
<tr>
<td>FFHT1p32v</td>
<td>Fast - Fast</td>
<td>125</td>
<td>1.32</td>
<td>High leakage corner</td>
</tr>
<tr>
<td>SSLT1p32v</td>
<td>Slow - Slow</td>
<td>-40</td>
<td>1.32</td>
<td>Low temperature corners</td>
</tr>
<tr>
<td>SSLT1p08v</td>
<td>Slow - Slow</td>
<td>-40</td>
<td>1.08</td>
<td></td>
</tr>
</tbody>
</table>

### Low Voltage Operating Conditions

<table>
<thead>
<tr>
<th>Corner Name</th>
<th>Process (NMOS proc. – PMOS proc.)</th>
<th>Temperature (T)</th>
<th>Power Supply (V)</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>TTNT0p80v</td>
<td>Typical - Typical</td>
<td>25</td>
<td>0.80</td>
<td>Typical corner</td>
</tr>
<tr>
<td>SSHT0p70v</td>
<td>Slow - Slow</td>
<td>125</td>
<td>0.70</td>
<td>Slow corner</td>
</tr>
<tr>
<td>FFLT0p90v</td>
<td>Fast - Fast</td>
<td>-40</td>
<td>0.90</td>
<td>Fast corner</td>
</tr>
<tr>
<td>FFHT0p90v</td>
<td>Fast - Fast</td>
<td>125</td>
<td>0.90</td>
<td>High leakage corner</td>
</tr>
<tr>
<td>SSLT0p90v</td>
<td>Slow - Slow</td>
<td>-40</td>
<td>0.90</td>
<td>Low temperature corners</td>
</tr>
<tr>
<td>SSLT0p70v</td>
<td>Slow - Slow</td>
<td>-40</td>
<td>0.70</td>
<td></td>
</tr>
</tbody>
</table>
DSCL: Additional Data

• Power / ground (PG) pin definitions are required for all cells in a library
  ▪ Defined as attributes in .lib
  ▪ Allows accurate definition of multiple power / ground pin information

• Benefits
  ▪ Power domain driven synthesis
  ▪ Automatic power net connections
  ▪ PST-based optimization
  ▪ Verification of PG netlist vs. power domains
  ▪ Power switch verification

pg_pin(VDD) {
  std_cell_main_rail : true ;
  voltage_name : VDD;
  pg_type : primary_power;
}
pg_pin(VSS) {
  voltage_name : VSS;
  pg_type : primary_ground;
}
DSCL: Power Verilog Models

- Power Verilog models
  - Separate verilog models with power modeling

```verilog
module AND2X1 (IN1, IN2, Q, VDD, VSS);
  output Q;
  input IN1, IN2;
  inout VDD;
  inout VSS;
  power_down iQ (Q, Qint, VDD, VSS);
  and (Qint, IN1, IN2);
endmodule

module AND2X1 (IN1, IN2, Q);
  output Q;
  input IN1, IN2;
  and (Q, IN2, IN1);
endmodule

primitive power_down (Q, Qint, VDD, VSS);
  output Q;
  input Qint, VDD, VSS;
  table
    | Qint | VDD | VSS |
    |------|-----|-----|
    | 0    | 0   | 0   |
    | 0    | 1   | 0   |
    | 0    | 1   | 1   |
    | 1    | 0   | 0   |
    | 1    | 1   | 0   |
    | 1    | 0   | 1   |
    | 1    | 1   | 1   |
    | x    | 0   | x   |
    | x    | 1   | x   |
    | x    | x   | x   |
endtable
endprimitive
```
DSCL: Special Cells for Low Power Techniques (1)

- **Power Gatings**
  - 5 cells with different loads
- **Always on**
  - 10 cells: 3 inverters, 3 buffers and 4 DFFs
- **Retention cells**
  - 44 cells negedge/posedge, scan
- **Isolation cells**
  - 8 cells with different logic, load
DSCL: Special Cells for Low Power Techniques (2)

- Level shifters
  - 16 cells Low/High, High/Low, with or without enable, with different loads
- Clock gatings:
  - 11 cells with different loads, edges, and control (post/pre)
- HVT Cells
  - All logical cells are designed using HVT, LVT
# DSCL: Special Cells for Low Power Techniques (3)

<table>
<thead>
<tr>
<th>Power Gates (MTCMOS)</th>
<th>Isolation Cells</th>
<th>Level Shifters</th>
<th>Retention Registers</th>
<th>Always On Logic</th>
</tr>
</thead>
<tbody>
<tr>
<td>Multiple Power Domains Single Voltage</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Multiple Voltage (MV) Domains</td>
<td></td>
<td>+</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Power Gating (shut down) Single Voltage No State Retention</td>
<td>+</td>
<td>+</td>
<td></td>
<td>+</td>
</tr>
<tr>
<td>MV Domains Power Gating No State Retention</td>
<td>+</td>
<td>+</td>
<td>+</td>
<td>+</td>
</tr>
<tr>
<td>MV Domains Power Gating State Retention</td>
<td>+</td>
<td>+</td>
<td>+</td>
<td>+</td>
</tr>
</tbody>
</table>

**Notes:**
- DSCL: Special Cells for Low Power Techniques
- MTCMOS: Multi-Threshold Complementary MOS
- MV: Multiple Voltage
- Power Gating: Shut down
- State Retention: + indicates presence
- Always On Logic: + indicates presence
Low Power Design of ChipTop Developed with DSCL: DC view
Low Power Design of ChipTop Developed with DSCL: ICC View
Conclusion

• Low Power Design requires significant design flow modifications
  ▪ UPF enables LPD flow automation
• Low Power design techniques have their huge impact on libraries
• SAED 90nm EDK DSCL includes all special cells needed for low power design techniques
• This 90nm EDK is currently in use in 235 universities of 37 countries
• This 90nm EDK is used inside Synopsys for education of customers

• Currently similar EDK is being developed for 32/28nm technology, initial release is planned in June 2011