Co-simulation Techniques for Mixed Signal Circuits

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Overview

• ASIC Development Flow
• Digital vs. Analog Verification
• Mixed Signal System Simulation
  – Analog Models
  – System Reference Models
• Example
  – Digital Air Pressure Sensor – Infineon
• Conclusions and Future Directions
• Questions and answers
ASIC Development Flow

Architecture development

Analog design

Digital design

Verification

Specs

Netlists

RTL Netlists

RTL
ASIC Development Flow

- **Functional verification:**
  - The task of proving that a design conforms to its specification and operates as required

- **Time spent on verification**
  - 71% of IC re-spins are due to functional bugs
  - 47% due to incorrect or incomplete specs
  - 60 – 70% of the development effort is in verification

Source: G. Bonfini, M. Chiavacci, R. Mariani, E. Pescari. Verification of Mixed Signal Systems
Digital vs. Analog Verification

• Random constrained stimulus generation vs. traditional directed testing

• Digital:
  – Functional correctness

• Analog:
  – Correct operation in all environmental conditions
Digital Verification

- Using HVLs: e, SystemVerilog
- Object oriented approach
- Increased level of abstraction

```verilog
task collect_serial()
  @(posedge vif.rx);
  #10;
  for(i = 15; i >= 0; i--) begin
    item.rx(i) = vif.rx;
    #10;
  end
end
```

```verilog```
packetGen()@ rdyToSend is {
  while(TRUE) {
    var packet : Packet;
    if sys.time - lastPacketTime >= 10 {
      gen packet;
      send(packet);
    } else {
      wait cycle;
    }
  }
}
```
Digital Verification

- “Random” stimulus
- Automatic checking
- Metrics to evaluate the results
- Verification plan
- Based on specs
  - no “white box” knowledge
- Improved reuse
- Methodologies – ERM, VMM, OVM, UVM
- Tools – logic simulators: QuestaSim, VCS, IUS
Analog verification

- Define input stimuli manually
- Visual inspection of waveforms
- File dumps of results
- Prone to error
- No clear metrics
- No unified methodology
- Detailed knowledge of the circuit necessary
- Tools: Nanosim, Ultrasim and Questa-ADMS
- Large simulation times

Mixed signal system simulation

- Bugs are usually found at the interactions between blocks
- Done using analog simulators
- Inherits weaknesses of analog verification
- Touch and feel approach
- Huge amount of simulation times
Mixed signal system simulation

Solution:

- Models for analog blocks
  - Capture only interesting behavior
  - Possibility to use logic simulators
    - Smaller simulation times
    - Plusses from digital verification
  - Languages:
    - Behavioral VHDL
    - Structural and mixed: Verilog AMS, VHDL AMS
Where the system level guys come in

• High level model of the system
  – C
  – SystemC
  – Simulink

• Architecture exploration, before the implementation phase
• Captures intended behavior
• Could be reused for verification
Where the system level guys come in

- **C and SystemC** supported by all major simulators
  - TLM support
  - Extensive methodologies

- **Matlab and Simulink**
  - Separate products for co-simulation
  - Interface at signal level
  - Licenses cost a lot of money
Example: Digital Air Pressure Sensor - Infineon
Conclusions and future directions

- Using models
  - Decreases testbench development time
  - Decreases simulation time (up to 1000x)
  - Allows to find bugs faster in the design cycle

- Multi-language testbenches -> UVM
- HVL testbenches for transistor level simulations
- Analog verification reuse
Thank you for your attention!

Questions and answers